

DATA SHEET

74ABT373A

Octal transparent latch (3-State)

Product specification

1995 Feb 17

IC23 Data Handbook

Octal transparent latch (3-State)

74ABT373A

FEATURES

- 8-bit transparent latch
- 3-State output buffers
- Output capability: +64mA/−32mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Power-up reset
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT373A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT373A device is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable (\overline{OE}) control gates.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable (\overline{OE}) controls all eight 3-State buffers independent of the latch operation.

When \overline{OE} is Low, the latched or transparent data appears at the outputs. When \overline{OE} is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

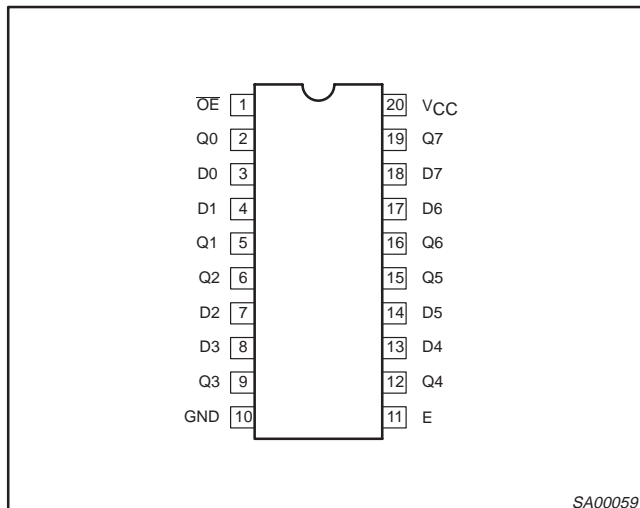
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	$C_L = 50\text{pF}; V_{CC} = 5\text{V}$	3.2 3.6	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; $V_O = 0\text{V}$ or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{CC} = 5.5\text{V}$	100	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	−40°C to +85°C	74ABT373A N	74ABT373A N	SOT146-1
20-Pin plastic SO	−40°C to +85°C	74ABT373A D	74ABT373A D	SOT163-1
20-Pin Plastic SSOP Type II	−40°C to +85°C	74ABT373A DB	74ABTD373A B	SOT339-1
20-Pin Plastic TSSOP Type I	−40°C to +85°C	74ABT373A PW	74ABT373APW DH	SOT360-1

PIN CONFIGURATION



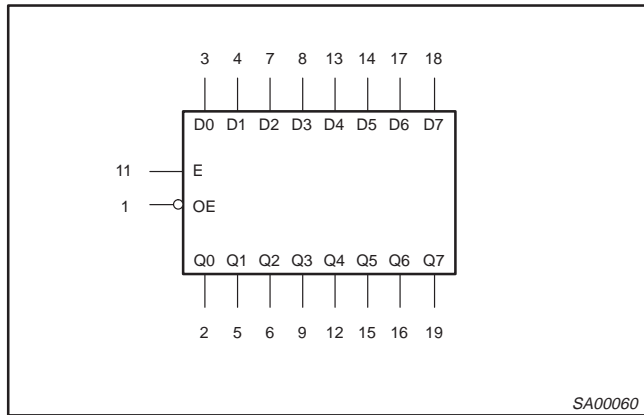
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	\overline{OE}	Output enable input (active-Low)
3, 4, 7, 8, 13, 14, 17, 18	D0-D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0-Q7	Data outputs
11	E	Enable input (active-High)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

Octal transparent latch (3-State)

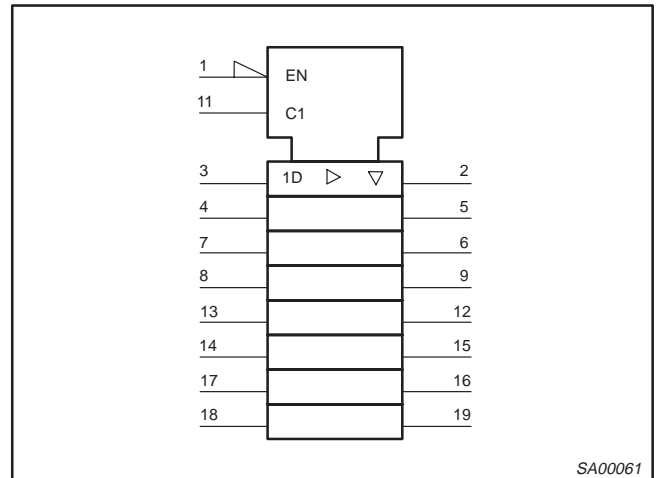
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LOGIC SYMBOL



SA00060

LOGIC SYMBOL (IEEE/IEC)



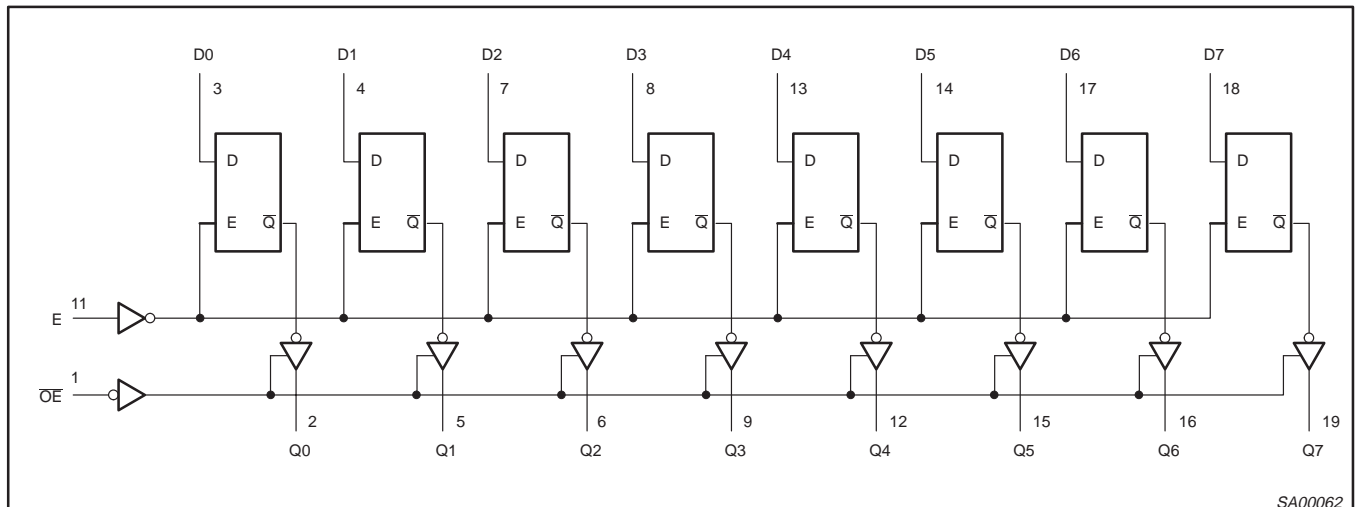
SA00061

FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
\overline{OE}	E	Dn		Q0 – Q7	
L	H	L	L	L	Enable and read register
L	H	H	H	H	
L	↓	l	L	L	Latch and read register
L	↓	h	H	H	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	Dn	Dn	Z	

- H = High voltage level
- h = High voltage level one set-up time prior to the High-to-Low E transition
- L = Low voltage level
- l = Low voltage level one set-up time prior to the High-to-Low E transition
- NC= No change
- X = Don't care
- Z = High impedance "off" state
- ↓ = High-to-Low E transition

LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	-18	mA
V _I	DC input voltage ³		-1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	output in Off or High state	-0.5 to +5.5	V
I _{OUT}	DC output current	output in Low state	128	mA
T _{stg}	Storage temperature range		-65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V _{CC}	DC supply voltage	4.5	5.5	V
V _I	Input voltage	0	V _{CC}	V
V _{IH}	High-level input voltage	2.0		V
V _{IL}	Low-level input voltage		0.8	V
I _{OH}	High-level output current		-32	mA
I _{OL}	Low-level output current		64	mA
Δt/Δv	Input transition rise or fall rate	0	5	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = -18mA		-0.9	-1.2		-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 4.5V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	2.5	2.9		2.5		V
		V _{CC} = 5.0V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	3.0	3.4		3.0		V
		V _{CC} = 4.5V; I _{OH} = -32mA; V _I = V _{IL} or V _{IH}	2.0	2.4		2.0		V
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}		0.3	0.55		0.55	V
V _{RST}	Power-up output low voltage ³	V _{CC} = 5.5V; I _O = 1mA; V _I = GND or V _{CC}		0.13	0.55		0.55	V
I _I	Input leakage current	V _{CC} = 5.5V; V _I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I _{OFF}	Power-off leakage current	V _{CC} = 0.0V; V _O or V _I ≤ 4.5V		±5.0	±100		±100	µA
I _{PU} /I _{PD}	Power-up/down 3-State output current	V _{CC} = 2.0V; V _O = 0.5V; $\overline{V_{OE}}$ = Don't Care V _I = GND or V _{CC}		±5.0	±50		±50	µA
I _{OZH}	3-State output High current	V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH}		0.1	50		50	µA
I _{OZL}	3-State output Low current	V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		-0.1	-50		-50	µA
I _{CEX}	Output High leakage current	V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}		5.0	50		50	µA
I _O	Output current ¹	V _{CC} = 5.5V; V _O = 2.5V	-50	-100	-180	-50	-180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}		100	250		250	µA
I _{CCL}		V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}		24	30		30	mA
I _{CCZ}		V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}		100	250		250	µA
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND		0.5	1.5		1.5	mA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

AC CHARACTERISTICS

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = -40 to +85°C V _{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Dn to Qn	2	1.4 1.4	3.2 3.6	4.2 4.7	1.4 1.4	4.7 5.1	ns
t _{PLH} t _{PHL}	Propagation delay E to Qn	1	1.4 1.9	3.2 3.7	4.2 4.8	1.4 1.9	4.8 5.1	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	4 5	1.2 2.1	3.1 4.2	4.2 5.2	1.2 2.1	5.1 5.7	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	4 5	1.3 1.2	3.4 3.0	4.6 4.1	1.3 1.2	5.1 4.3	ns

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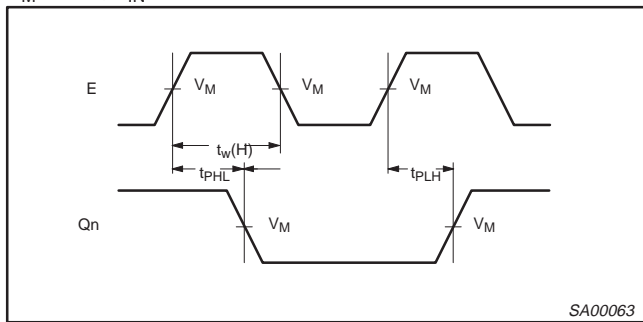
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

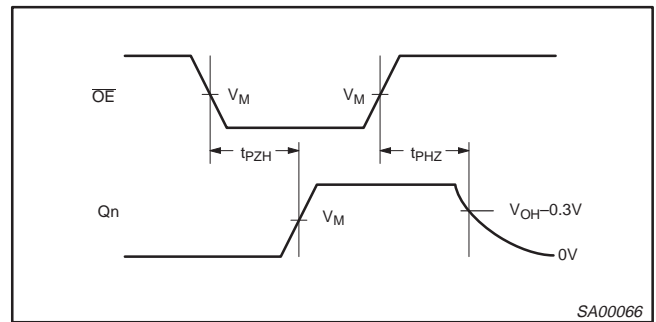
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$		$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$	
			Min	Typ	Min	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low Dn to E	3	1.5 1.0	0.7 0.4	1.5 1.0	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low Dn to E	3	1.0 1.0	0.0 -0.5	1.0 1.0	ns
$t_w(\text{H})$	E pulse width High	1	2.5	1.7	2.5	ns

AC WAVEFORMS

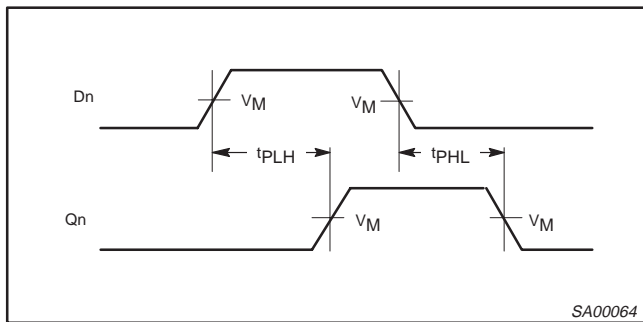
$V_M = 1.5\text{V}$, $V_{\text{IN}} = \text{GND to } 3.0\text{V}$



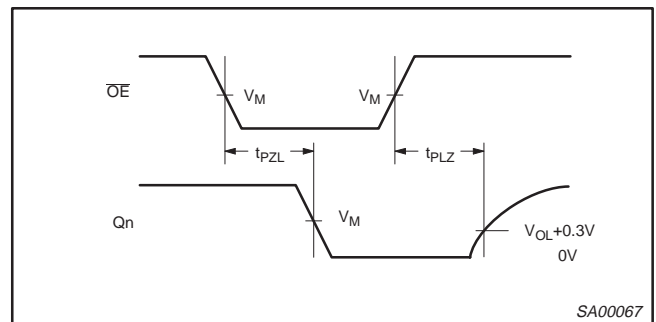
Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width



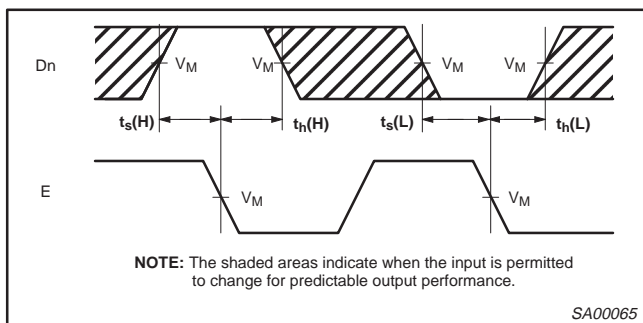
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 2. Propagation Delay for Data to Outputs



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

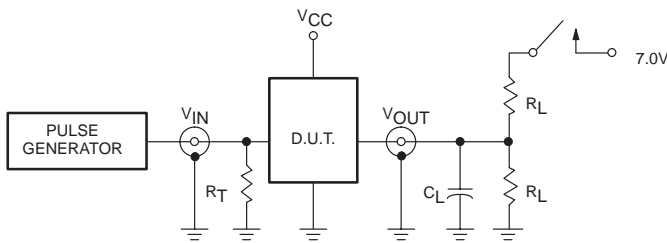


Waveform 3. Data Setup and Hold Times

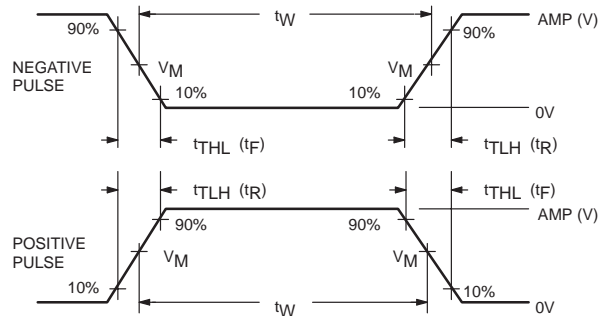
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TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal transparent latch (3-State)**74ABT373A**

DIP20: plastic dual in-line package; 20 leads (300 mil)**SOT146-1****SO20: plastic small outline package; 20 leads; body width 7.5 mm****SOT163-1**

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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

Octal transparent latch (3-State)

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

Octal transparent latch (3-State)

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DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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