

## Field Programmable Blank Oscillator

Series **CPPL**

- Programmed with the PG-2000P, PG-3000 field oscillator programming instrument within seconds
- Can be programmed twice
- Provides a sealed finished custom oscillator
- Standard Package Options
- Ultra low jitter @ 1 million samples
- Power down and Tri-State options



**Part Numbering Example: CPPL C 1 L Z - A5 B6 - XX.XXXX TS**

CPPL	C	1	L	Z	A5	B6	XX.XXXX	TS
SERIES	OUTPUT	PACKAGE STYLE	VOLTAGE	ADDED FEATURES	OPERATING TEMP.	STABILITY	FREQUENCY	TRI-STATE
CPPL	C = CMOS T = TTL	1 = Full Size 4 = Half Size 5 = 3.2X5 Ceramic 7 = 5X7 Ceramic 8 = PLASTIC SMD	Blank = 5V L = 3.3 V	Blank = Bulk T = Tube Z = Tape and Reel	Blank = 0°C +70°C A5 = -20°C +70°C A7 = -40°C +85°C	B6 = ±100 ppm BP = ±50 ppm BR = ±25 ppm	1.000-133.000 MHz	TS = Tri-State PD=PowerDwn

### Specifications:

Description	Min	Typ	Max	Unit
<b>Frequency Range:</b> Programmable to Any Discrete Frequency	1.000		133.000	MHz
<b>Available Stability Options:</b>	-100 -50 -25		100 50 25	ppm ppm ppm
<b>Programmable Input Voltage:</b> (1-133 MHz) (1-100 MHz)	4.5 3.0	5.0 3.3	5.5 3.6	V V
<b>Operating Temperature Range Options:</b>	0 -20 -40		+70 +70 +85	°C °C °C
<b>Storage Temperature:</b>	-55		+125	°C
Aging (PPM/Year) Ta=25C, Vdd=5/3.3V			±5	
<b>Programmable Output Level:</b>	TTL/CMOS			
<b>Packaging:</b>	Tape and Reel (1K per Reel) Tube Bulk Shipping			

### Operating Load Conditions:

Description	Min	Max	Unit
Vdd Supply Voltage	3.0	5.5	V
CTTL Max Capacitive Load on outputs for TTL levels 4.5V-5.5V Vdd ≤ 40 MHz 4.5V-5.5V Vdd > 40-133 MHz		50	pF
		25	pF
CCMOS Max Capacitive Load on outputs for CMOS levels 4.5V-5.5V Vdd, ≤ 66 MHz 4.5V-5.5V Vdd, >66-133 MHz 3.0V-3.6V Vdd, ≤ 40 MHz 3.0V-3.6V Vdd, >40-100 MHz		50	pF
		25	pF
		30	pF
		15	pF



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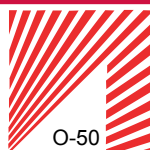
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### Electrical Characteristics

Description	TEST CONDITIONS	Min	Typ	Max	Unit
<b>Input Characteristics (Pin 1):</b>					
V <sub>IL</sub> , Low-Level Input Voltage TO TRI-STATE OR POWER DOWN	4.5–5.5V V <sub>dd</sub> 3.0–3.6V V <sub>dd</sub>			0.8 0.2V <sub>dd</sub>	V V
V <sub>IH</sub> , High-Level Input Voltage TO ENABLE OUTPUT OR open	4.5–5.5V V <sub>dd</sub> 3.0–3.6V V <sub>dd</sub>	2.0 0.7 V <sub>dd</sub>			V V
I <sub>IL</sub> , Input Low Current I <sub>IH</sub> , Input High Current	V <sub>IN</sub> = 0V V <sub>IN</sub> = V <sub>dd</sub>			10 5	μA μA
<b>Output Characteristics:</b>					
V <sub>OL</sub> , Low-Level Output Voltage	4.5V–5.5V V <sub>dd</sub> , 16 mA I <sub>oL</sub> 3.0V–3.6V V <sub>dd</sub> , 8 mA I <sub>oL</sub>			0.4 0.4	V V
V <sub>OHTTL</sub> , High-level Output Voltage TTL	4.5V–5.5V V <sub>dd</sub> , -16 mA I <sub>oL</sub>	2.4			V
V <sub>OHCMS</sub> , High-level CMOS Voltage	4.5V–5.5V V <sub>dd</sub> , -16 mA I <sub>oL</sub> 3.0V–3.6V V <sub>dd</sub> , -8 mA I <sub>oL</sub>	V <sub>dd</sub> -0.4 V <sub>dd</sub> -0.4			V V
<b>Power Supply Current: (unloaded)</b>	4.5–5.5 V <sub>dd</sub> , OUTPUT FREQ ≤ 133 MHz 3.0–3.6 V <sub>dd</sub> , OUTPUT FREQ ≤ 100 MHz			45 25	mA mA
<b>Standby Current:</b>			10	50	μA
<b>Tristate pull up</b>	4.5–5.5 V <sub>dd</sub> , V <sub>IN</sub> = 0V 4.5–5.5 V <sub>dd</sub> , V <sub>IN</sub> = 0.7V	1.1 50	3.0 100	8.0 200	MΩ KΩ
<b>Tri-State Leakage Current</b>	5.0 V <sub>dd</sub>		20		μA
<b>Output Enable Mode:</b>	Output is Tri-Stated				
<b>Power Down Mode:</b>	Output is Tri-Stated.				

"Tristate internal pull up. Output active when high"



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## Output Clock Switching Characteristics

Description	TEST CONDITIONS	Min	Typ	Max	Unit
<b>Duty Cycle:</b> TTL @ 1.4 V 4.5-5.5 Vdd	≤ 50 MHz, C <sub>L</sub> = 50 pF	45		55	%
	50–66 MHz, C <sub>L</sub> = 15 pF	45		55	%
	66–125 MHz, C <sub>L</sub> = 25 pF	40		60	%
	125–133 MHz, C <sub>L</sub> = 15 pF	40		60	%
<b>Duty Cycle:</b> CMOS @ Vdd/2 4.5-5.5 Vdd 3.0–3.6 Vdd	≤ 66 MHz, C <sub>L</sub> ≤ 25 pF	45		55	%
	66–125 MHz, C <sub>L</sub> ≤ 25 pF	40		60	%
	125–133 MHz, C <sub>L</sub> ≤ 15 pF	40		60	%
	≤ 40 MHz, C <sub>L</sub> ≤ 30 pF	45		55	%
	40-100 MHz, C <sub>L</sub> ≤ 15 pF	40		60	%
<b>Output Clock Rise/Fall</b>	0.8V–2.0V, 4.5-5.5 Vdd, C <sub>L</sub> = 50			1.8	ns
	0.8V–2.0V, 4.5-5.5 Vdd, C <sub>L</sub> = 25			1.2	ns
	0.8V–2.0V, 4.5-5.5 Vdd, C <sub>L</sub> = 15			0.9	ns
	0.2–0.8Vdd, 4.5-5.5 Vdd, C <sub>L</sub> = 50			3.4	ns
	0.2–0.8Vdd, 3.0–3.6 Vdd, C <sub>L</sub> = 30			4.0	ns
	0.2–0.8Vdd, 3.0–3.6 Vdd, C <sub>L</sub> = 15			2.4	ns
<b>Start Up Time</b>	From power on			2	ms
<b>Power Down Delay Time</b> Synchronous Asynchronous	PWR_DWN pin LOW to output Hi-Z		T/2	T+10	ns
			10	15	ns
<b>Output Disable Time</b> Synchronous Asynchronous	OE pin LOW to output Hi-Z T = Frequency oscillator period		T/2	T+10	ns
			10	15	ns
<b>Output Enable Time</b>			<b>T</b>	<b>1.5 T + 25</b>	<b>ns</b>
<b>RMS Period Jitter:</b> Peak to Peak *	1 – 133 MHz		8	11	ps
	≤ 33.000 MHz > 33.000 MHz		65 65	99 80	ps ps

\* Jitter tested at > 1,000,000 samples, exceeding JEDEC std JESD65.

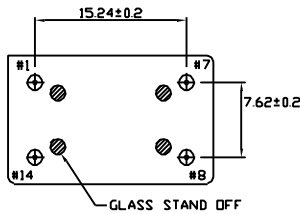
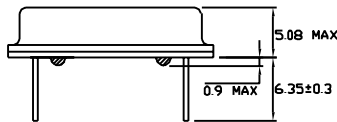
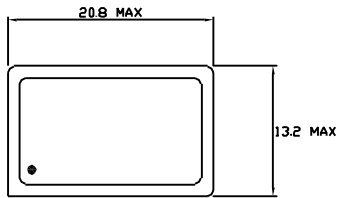


# Field Programmable Blank Oscillator

Note: Bypass Vdd to GND with a 0.01  $\mu$ F capacitor

## Style 1 Full Size 14 Pin Dip

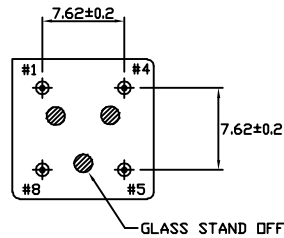
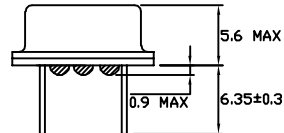
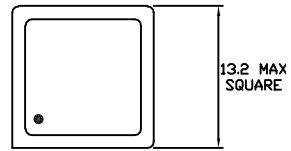
STYLE 1 FULL SIZE 14 PIN DIP



**PIN FUNCTION**  
 1 CONTROL  
 7 GND  
 8 OUTPUT  
 14 Vdd

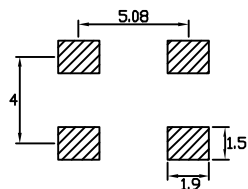
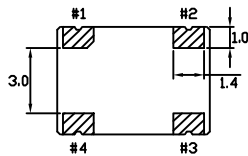
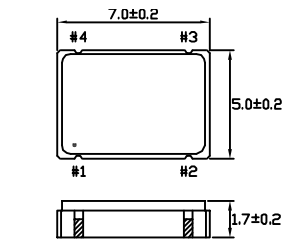
## Style 4 Half Size 8 Pin Dip

STYLE 4 HALFSIZE 8 PIN DIP



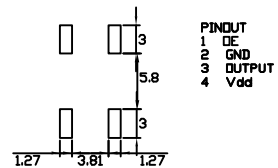
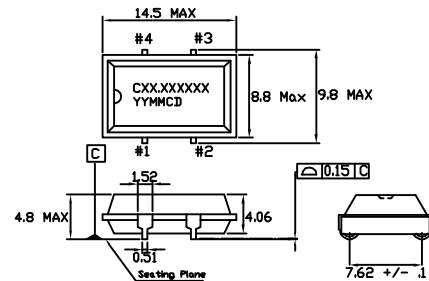
**PIN FUNCTION**  
 1 CONTROL  
 4 GND  
 5 OUTPUT  
 8 Vdd

## Style 7 5x7 Ceramic SMD



**PIN FUNCTION**  
 1 CONTROL  
 2 GND  
 3 OUTPUT  
 4 Vdd

## Style 8 Plastic SMD



**PINOUT**  
 1 OE  
 2 GND  
 3 OUTPUT  
 4 Vdd

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*Note: Bypass Vdd to GND with a 0.01  $\mu$ F capacitor*

## Style 5 3.2x5 Ceramic SMD

