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The MPC850 is a versatile, one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications, excelling particularly in communications and networking products. The MPC850 is specifically designed for cost-sensitive remote-access applications such as ADSL modems, cable modems, and SOHO routers. It provides functions similar to the MPC860 with the addition of universal serial bus (USB) support.

The MPC850 is compliant with the PowerPC architecture. It also integrates system functions such as a versatile memory controller and a communications processor module (CPM) that incorporates a specialized, independent RISC communications processor. This separate processor off-loads peripheral tasks from the MPC8xx core.

The MPC850 CPM supports up to seven serial channels, as follows:

- Two serial communications controllers (SCCs). The SCCs support Ethernet, ATM HDLC and a number of other protocols, along with a transparent mode of operation. Up to 64 logical HDLC channels can be supported on a single SCC.

- One USB channel

- Two serial management controllers (SMCs)

- One I^2C port

- One serial peripheral interface (SPI)

Table 1 shows the functionality supported by the members of the MPC850 family.

Table 1. MPC850 Functionality Matrix

Part	USB Support	SCC Support	ATM Support
MPC850	One USB port	One SCC (SCC2) - includes Ethernet support	—
MPC850DE	One USB port	Two SCCs; both support Ethernet	—
MPC850SR	One USB port	Two SCCs: both support Ethernet, multi-channel HDLC, and serial ATM	UTOPIA interface
MPC850DSL	One USB port	SCC2 supports Ethernet only, SCC3 supports UART only. I^2C is not supported.	UTOPIA interface

Additional documentation may be provided for parts listed in Table 1.

1.1 Features

Figure 1 is a block diagram of the MPC850, showing its major components and the relationships among those components.
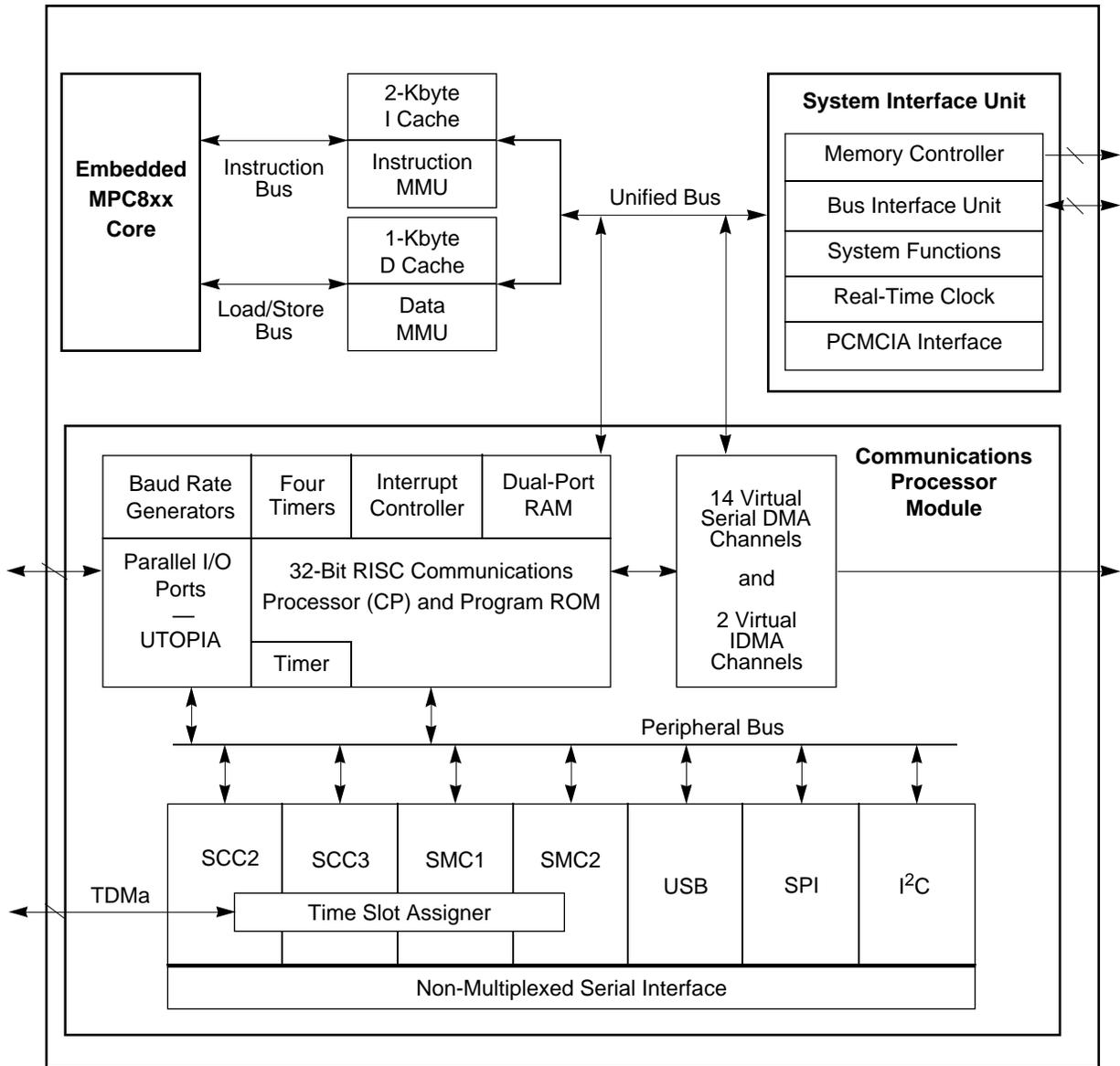

Figure 1. MPC850 Microprocessor Block Diagram

The following list summarizes the main features of the MPC850.

- MPC8xx core
  - Single-issue, 32-bit core (fully compatible with PowerPC user instruction set architecture definition) with 32 x 32-bit integer registers
  - Performs branch folding and branch prediction with conditional prefetch, but without conditional execution
  - 2-Kbyte data cache and 1-Kbyte instruction cache (Harvard architecture)
    - Caches are two-way, set-associative

- – Physically addressed
- – Cache blocks can be updated with a 4-word line burst
- – Least-recently used (LRU) replacement algorithm
- – Lockable one-line granularity
- — Memory management units (MMUs) with 8-entry translation lookaside buffers (TLBs) and fully-associative instruction and data TLBs
- — MMUs support multiple page sizes of 4 Kbytes, 16 Kbytes, 256 Kbytes, 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and eight protection groups
- Advanced on-chip emulation debug mode
- Data bus dynamic bus sizing for 8-, 16-, and 32-bit buses
  - — Supports traditional 68000 big-endian, traditional x86 little-endian and modified little-endian memory systems
  - — Twenty-six external address lines
- Completely static design (0–80 MHz operation)
- System integration unit (SIU)
  - — Hardware bus monitor
  - — Spurious interrupt monitor
  - — Software watchdog
  - — Periodic interrupt timer
  - — Low-power stop mode
  - — Clock synthesizer
  - — Decrementer
  - — Real-time clock and time base
  - — Reset controller
  - — IEEE 1149.1 test access port (JTAG)
- Memory controller (eight banks)
  - — Glueless interface to DRAM single in-line memory modules (SIMMs), synchronous DRAM (SDRAM), static random-access memory (SRAM), electrically programmable read-only memory (EPROM), flash EPROM, etc.
  - — Memory controller programmable to support most size and speed memory interfaces
  - — Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - — Variable block sizes, 32 Kbyte to 256 Mbyte
  - — Selectable write protection
  - — On-chip bus arbitration supports external bus master
  - — Special features for burst mode support
- General-purpose timers
  - — Four 16-bit timers or two 32-bit timers
  - — Gate mode can enable/disable counting
  - — Interrupt can be masked on reference match and event capture
- Interrupts
  - — Eight external interrupt request (IRQ) lines
  - — Twelve port pins with interrupt capability

- — Fifteen internal interrupt sources
- — Programmable priority among SCCs and USBs
- — Programmable highest-priority request
- Single socket PCMCIA-ATA interface
  - — Master (socket) interface, release 2.1 compliant
  - — Single PCMCIA socket
  - — Supports eight memory or I/O windows
- Communications processor module (CPM)
  - — 32-bit, Harvard architecture, scalar RISC communications processor (CP)
  - — Protocol-specific command sets (for example, GRACEFUL STOP TRANSMIT stops transmission after the current frame is finished or immediately if no frame is being sent and CLOSE RXBD closes the receive buffer descriptor)
  - — Up to 384 buffer descriptors (BDs)
  - — Supports continuous mode transmission and reception on all serial channels
  - — Up to 8 Kbytes of dual-port RAM
  - — Fourteen serial DMA (SDMA) channels
  - — Three parallel I/O registers with open-drain capability
- Four independent baud-rate generators (BRGs)
  - — Can be connected to any SCC, SMC, or USB
  - — Allow changes during operation
  - — Autobaud support option
- Two SCCs (serial communications controllers)
  - — Ethernet/IEEE 802.3, supporting full 10-Mbps operation
  - — HDLC/SDLC™ (all channels supported at 2 Mbps)
  - — HDLC bus (implements an HDLC-based local area network (LAN))
  - — Asynchronous HDLC to support PPP (point-to-point protocol)
  - — AppleTalk™
  - — Universal asynchronous receiver transmitter (UART)
  - — Synchronous UART
  - — Serial infrared (IrDA)
  - — Totally transparent (bit streams)
  - — Totally transparent (frame based with optional cyclic redundancy check (CRC))
- QUICC multichannel controller (QMC) microcode features
  - — Up to 64 independent communication channels on a single SCC
  - — Arbitrary mapping of 0–31 channels to any of 0–31 TDM time slots
  - — Supports either transparent or HDLC protocols for each channel
  - — Independent TxBDs/Rx and event/interrupt reporting for each channel
- Two serial management controllers (SMCs)
  - — UART
  - — Transparent
  - — General circuit interface (GCI) controller

— Can be connected to the time-division-multiplexed (TDM) channel

- One serial peripheral interface (SPI)
  - Supports master and slave modes
  - Supports multimaster operation on the same bus
- One I^{2}C$^®$ (interprocessor-integrated circuit) port
  - Supports master and slave modes
  - Supports multimaster environment
- Time slot assigner
  - Allows SCCs and SMCs to run in multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user-defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame syncs, clocking
  - Allows dynamic changes
  - Can be internally connected to four serial channels (two SCCs and two SMCs)
- Low-power support
  - Full high: all units fully powered at high clock frequency
  - Full low: all units fully powered at low clock frequency
  - Doze: core functional units disabled except time base, decrementer, PLL, memory controller, real-time clock, and CPM in low-power standby
  - Sleep: all units disabled except real-time clock and periodic interrupt timer. PLL is active for fast wake-up
  - Deep sleep: all units disabled including PLL, except the real-time clock and periodic interrupt timer
  - Low-power stop: to provide lower power dissipation
  - Separate power supply input to operate internal logic at 2.2 V when operating at or below 25 MHz
  - Can be dynamically shifted between high frequency (3.3 V internal) and low frequency (2.2 V internal) operation
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - The MPC850 can compare using the =, , <, and > conditions to generate watchpoints
  - Each watchpoint can generate a breakpoint internally
- 3.3-V operation (No support for 5V I/O)

1.2   Overview

As shown in Figure 1, the MPC850 adopts a dual-processor design, providing a high-performance MPC8xx core for application programming use and a communications processor module that contains a special-purpose 32-bit scalar RISC communications processor (CP).

Components of the *MPC850 Integrated Communications Microprocessor User's Manual* are described in the following sections following the organizational structure of this manual.

- Part II, "MPC8xx core Microprocessor Module," describes the MPC8xx microprocessor core embedded in the MPC850. These chapters provide details concerning the processor core as it implements the PowerPC architecture.
- Part III, "Configuration and Reset," describes start-up behavior of the MPC850.
- Part IV, "The Hardware Interface," describes external signals, clocking, memory control, and power management of the MPC850.
- Part V, "Communications Processor Module," describes the configuration, clocking, and operation of the various communications protocols supported by the MPC850.
- Part VI, "System Debugging and Testing Support," describes how to use the MPC850 facilities for debugging and system testing.

1.3 MPC8xx Microprocessor Module

The MPC8xx core is a fully-static design. It executes all integer and load/store operations directly on the hardware. The core supports integer operations on a 32-bit internal data path and 32-bit arithmetic hardware. Its interface to the internal and external buses is 32 bits. The core uses a two-instruction load/store queue, four-instruction prefetch queue, and a six-instruction history buffer.

The core performs branch folding and branch prediction with conditional prefetch, but without conditional execution. The core can operate on 32-bit external operands with one bus cycle. The integer block supports thirty-two 32-bit general-purpose registers (GPRs), which are used as source and destination operands for instruction execution.

The integer unit typically can execute one integer instruction on each clock cycle. Each element in the integer block is clocked only when valid data is present in the data queue and ready for operation, which reduces power consumption to the amount needed for an operation.

The core processor is integrated with the MMUs and 2-Kbyte instruction and 1-Kbyte data caches. The MMUs provide an 8-entry, fully-associative instruction and data TLB, with multiple page sizes of 4 Kbytes (1-Kbyte protection), 16 Kbytes, 512 Kbytes, and 8 Mbytes. It supports 16 virtual address spaces with eight protection groups. Three special-purpose registers are provided to support software table searching and updating page translations.

The 2-Kbyte instruction cache is two-way, set associative with physical addressing. It allows single-cycle access on hits with no added latency for miss. It has four words per line and supports burst linefill using an LRU replacement algorithm. The instruction cache can be locked on a line-by-line basis for application-critical routines.

The 1-Kbyte data cache is two-way, set associative with physical addressing. It allows single-cycle access on hit with one added clock latency for miss. It has four words per line and supports burst linefill using an LRU replacement algorithm. The data cache can also be locked on a line-by-line basis for application-critical routines. It can be programmed to support copy-back or write-through via the MMU. Cache-inhibit mode can be programmed on a per-page basis.

1.4 Configuration and Reset

The MPC850 configuration is handled through the system interface unit (SIU), which is described in Section 1.4.1, "System Interface Unit (SIU)." The MPC850 provides many different kinds of reset, as described in Section 1.4.2, "Resets."

1.4.1 System Interface Unit (SIU)

The SIU controls system start-up, initialization, operation, protection, and the external system bus. The system configuration and protection function controls the overall system and provides various monitors and timers, including the bus monitor, software watchdog timer, periodic interrupt timer (PIT), decrementer, timebase, and real-time clock. The clock synthesizer generates the clock signals for other modules and external devices that the SIU interfaces with. The SIU supports various low-power modes that supply different ranges of power consumption, functionality, and wake-up time. The clock scheme supports low-power modes for applications that use baud rate generators and/or serial ports in standby mode. The main system clock can be changed dynamically; the baud rate generators and serial ports work with a fixed frequency.

Although the MPC8xx core is a 32-bit device internally, it can be configured to operate with an 8-, 16-, or 32-bit data bus. Regardless of system bus size, dynamic bus sizing is supported, which allows 8-, 16-, and 32-bit peripherals and memory to coexist on the 32-bit system bus. The SIU supports traditional 68000 big-endian memory systems, traditional x86 little-endian memory systems, and modified little-endian memory systems.

The memory controller supports up to eight memory banks with glueless interfaces to DRAM, SRAM, PSRAM, EPROM, flash EPROM, SDRAM, EDO, and other peripherals with two-clock initial access to external SRAM and bursting support. It provides variable block sizes from 32 Kbytes to 256 Mbytes. The memory controller provides 0 to 15 wait states for each bank of memory and can use address type matching to qualify each memory bank access. It provides four byte-enable signals for varying width devices, one output enable signal, and one boot chip-select available at reset.

The DRAM interface supports 8-, 16-, and 32-bit ports. It uses a programmable state machine to support almost any memory interface. Memory banks can be defined in depths of 256 or 512 Kbytes or 1, 2, 4, 8, 16, 32, or 64 Mbytes for all port sizes. In addition, the memory depth can be defined as 64 Kbytes and 128 Kbytes for 8-bit memory or 128 Mbytes and 256 Mbytes for 32-bit memory. The DRAM controller supports page mode access for successive transfers within bursts. The MPC850 supports a glueless interface to one bank of DRAM, while external buffers are required for additional memory banks. The refresh unit provides $\overline{CAS}$ before $\overline{RAS}$, a programmable refresh timer, active refresh during external reset, the ability to disable refresh, and stacking for a maximum of seven refresh cycles.

The PCMCIA-ATA interface is a master controller that is compliant with release 2.1. The interface supports one independent PCMCIA socket with external transceivers or buffers required. It provides eight memory or I/O windows that can be allocated to the socket. If the PCMCIA port is not being used as a card interface, it can be used as a general-purpose input with interrupt capability.

1.4.2 Resets

The reset block has reset control logic that determines the cause of reset, synchronizes it if necessary, and resets the appropriate logic modules. The memory controller, system protection logic, interrupt controller, and parallel I/O signals are initialized only on hard reset. Soft reset initializes the internal logic while maintaining the system configuration.

The MPC850 has several sources of input to the reset logic:

- Power-on reset
- External hard reset
- Internal hard reset
  - Loss of lock

— Software watchdog reset

— Checkstop reset

— Debug port hard reset

- JTAG reset

- External soft reset

- Internal soft reset (debug port soft reset)

All of these reset sources are fed into the reset controller and, depending on the source of the reset, different actions are taken. The reset status register reflects the last source to cause a reset.

1.5   MPC850 Hardware Interface

The MPC850 bus is a synchronous, burstable bus that can support multiple masters. Signals driven on this bus are required to make the setup and hold time relative to the bus clock's rising edge. The MPC850 architecture supports byte, half-word, and word operands allowing access to 8-, 16-, and 32-bit data ports through the use of synchronous cycles controlled by the size outputs (TSIZ0, TSIZ1). Access to 16- and 8-bit ports is done for slaves controlled by the memory controller.

The MPC850 bus interface features are as follows:

- 26-bit address bus with transfer size indication

- 32-bit data bus

- Dynamic bus sizing to 32-, 16-, or 8-bit ports accessed through the memory controller

- TTL-compatible interface

- Bus arbitration supported optionally by internal or external logic

- Bus arbitration logic on-chip supports an external master with programmable priority

- Compatible with PowerPC architecture

- Easy to interface to slave devices

- Bus is synchronous (all signals are referenced to rising edge of bus clock)

- Contains support for data parity

The PCMCIA host adapter module provides all control logic for a PCMCIA socket interface, and requires only additional external analog power switching logic and buffering.

1.5.1   Signals

Figure 2 shows MPC850 signals grouped by function. Note that many of these signals are multiplexed and this figure does not indicate how these signals are multiplexed.

NOTE

A bar over a signal name indicates that the signal is active low—for example, $\overline{BB}$ (bus busy). Active-low signals are referred to as asserted (active) when they are low and negated when they are high. Signals that are not active low, such as TSIZ[0–1] (transfer size signals) are referred to as asserted when they are high and negated when they are low.
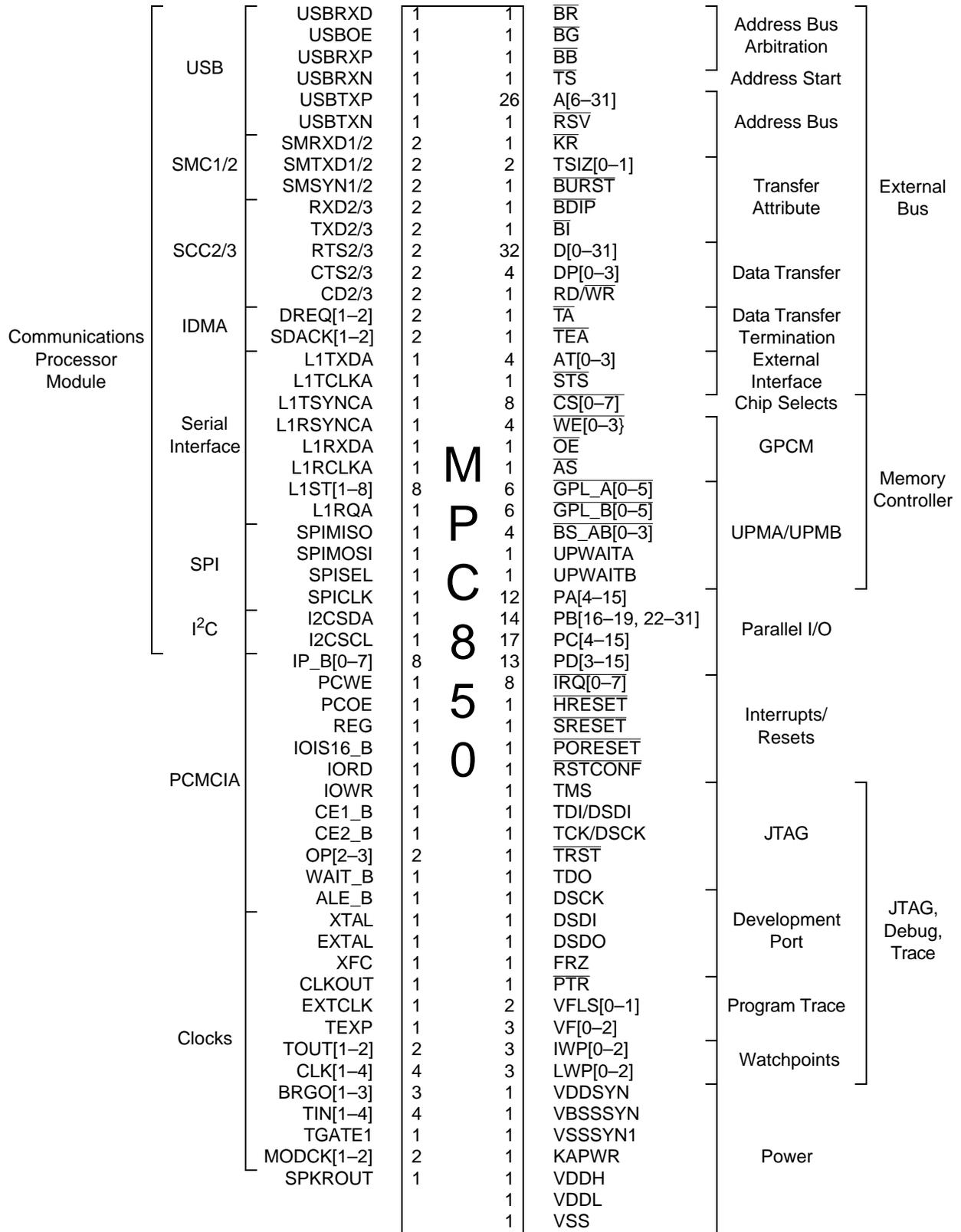
Module	Signal	#	#	Signal	Group	
	USBRXD	1	1	$\overline{BR}$	Address Bus Arbitration	
USB	USBOE	1	1	$\overline{BG}$		
	USBRXP	1	1	$\overline{BB}$		
	USBRXN	1	1	$\overline{TS}$	Address Start	
	USBTXP	1	26	A[6–31]		
	USBTXN	1	1	$\overline{RSV}$	Address Bus	
SMC1/2	SMRXD1/2	2	1	$\overline{KR}$		
	SMTXD1/2	2	2	TSIZ[0–1]		
	SMSYN1/2	2	1	$\overline{BURST}$	Transfer Attribute	External Bus
	RXD2/3	2	1	$\overline{BDIP}$		
	TXD2/3	2	1	$\overline{BI}$		
SCC2/3	RTS2/3	2	32	D[0–31]		
	CTS2/3	2	4	DP[0–3]	Data Transfer	
	CD2/3	2	1	RD/$\overline{WR}$		
IDMA	DREQ[1–2]	2	1	$\overline{TA}$	Data Transfer Termination	
	SDACK[1–2]	2	1	$\overline{TEA}$		
	L1TXDA	1	4	AT[0–3]	External Interface	
	L1TCLKA	1	1	$\overline{STS}$		
	L1TSYNCA	1	8	$\overline{CS[0–7]}$	Chip Selects	
Serial Interface	L1RSYNCA	1	4	$\overline{WE[0–3]}$		
	L1RXDA	1	1	$\overline{OE}$	GPCM	
	L1RCLKA	1	1	$\overline{AS}$		Memory Controller
	L1ST[1–8]	8	6	$\overline{GPL\_A[0–5]}$		
	L1RQA	1	6	$\overline{GPL\_B[0–5]}$		
	SPIMISO	1	4	$\overline{BS\_AB[0–3]}$	UPMA/UPMB	
SPI	SPIMOSI	1	1	UPWAITA		
	SPISEL	1	1	UPWAITB		
	SPICLK	1	12	PA[4–15]		
I²C	I2CSDA	1	14	PB[16–19, 22–31]	Parallel I/O	
	I2CSCL	1	17	PC[4–15]		
	IP_B[0–7]	8	13	PD[3–15]		
	PCWE	1	8	$\overline{IRQ[0–7]}$		
	PCOE	1	1	$\overline{HRESET}$		
	REG	1	1	$\overline{SRESET}$	Interrupts/ Resets	
	IOIS16_B	1	1	$\overline{PORESET}$		
PCMCIA	IORD	1	1	$\overline{RSTCONF}$		
	IOWR	1	1	TMS		
	CE1_B	1	1	TDI/DSDI		
	CE2_B	1	1	TCK/DSCK	JTAG	
	OP[2–3]	2	1	$\overline{TRST}$		
	WAIT_B	1	1	TDO		
	ALE_B	1	1	DSCK		
	XTAL	1	1	DSDI	Development Port	JTAG, Debug, Trace
	EXTAL	1	1	DSDO		
	XFC	1	1	FRZ		
	CLKOUT	1	1	$\overline{PTR}$		
	EXTCLK	1	2	VFLS[0–1]	Program Trace	
	TEXP	1	3	VF[0–2]		
Clocks	TOUT[1–2]	2	3	IWP[0–2]	Watchpoints	
	CLK[1–4]	4	3	LWP[0–2]		
	BRGO[1–3]	3	1	VDDSYN		
	TIN[1–4]	4	1	VBSSSYN		
	TGATE1	1	1	VSSSYN1		
	MODCK[1–2]	2	1	KAPWR	Power	
	SPKROUT	1	1	VDDH		
			1	VDDL		
			1	VSS		

Communications Processor Module — MPC850

Figure 2. MPC850 Functional Signal Diagram

1.5.2 Clocking and Power Management

The MPC850 clock system provides many different clocking options for all on-chip and external devices. For its clock sources, the MPC850 contains phase-locked loop and crystal oscillator support circuitry. The phase-locked loop circuitry can be used to provide a high-frequency system clock from a low-frequency external source. Also, to enable flexible power control, the MPC850 provides frequency dividers and a variety of low-power mode options.

The MPC850 allows a system to optimize power utilization by providing performance on-demand. This is implemented through a variety of programmable power-saving modes with automatic wake-up features.

The main features of the MPC850 clocks and power control system are as follows:

- Contains system PLL (SPLL)
- Supports crystal oscillator circuits
- Clock dividers are provided for low-power modes and internal clocks
- Contains five major power-saving modes
    - Normal (high and low)
    - Doze (high and low)
    - Sleep
    - Deep sleep
    - Power down

The MPC850 supports a wide range of power management features including full-high, full-low, doze, sleep, deep-sleep, and low-power stop. These modes progressively reduce power consumption, as follows:

- In full-high mode, the MPC850 is fully powered with all internal units operating at the full processor speed.
- Full-low mode is the same as full-high, but operates at a lower frequency. A gear mode determined by a clock divider allows the operating system to reduce the operational frequency of the processor.
- Doze mode disables core functional units except the time base, decrementer, PLL, memory controller, real-time clock, and places the CPM in low-power standby mode.
- Sleep mode is the next lower power mode. It disables everything except the real-time clock and periodic interrupt timer, leaving the PLL active for quick wake-up.
- Deep-sleep mode disables the PLL for lower power, but slower wake-up.
- Low-power stop disables all logic in the processor except the minimum logic required to restart the device, and provides the lowest power consumption but requires the longest wake-up time.

1.5.3 Memory Controller

The memory controller is responsible for controlling a maximum of eight memory banks shared between a general-purpose chip-select machine (GPCM) and a pair of sophisticated user-programmable machines (UPMs). It supports a glueless interface to SRAM, EPROM, flash EPROM, regular DRAM devices, self-refresh DRAMs, extended data output DRAM devices, synchronous DRAMs, and other peripherals. This flexible memory controller allows the implementation of memory systems with very specific timing requirements.

The GPCM provides interfacing for simpler, lower-performance memory resources and memory-mapped devices. The GPCM has inherently lower performance because it does not support bursting. For this reason,

GPCM-controlled banks are used primarily for boot-loading and access to nonburstable memory-mapped peripherals.

The UPM provides both more features and, because it supports bursting, higher performance. Therefore it is typically used to interface with higher-performance run-time memory such as DRAM and bursting SRAM.

The UPM supports address multiplexing of the external bus, periodic timers, and generation of programmable control signals for row address and column address strobes to allow for a glueless interface to DRAM devices. The periodic timers allow refresh cycles to be initiated while the address multiplexing provides row and column addresses.

Different timing patterns can be generated for the control signals that govern a memory device. These patterns define how the external control signals behave in read-access, write-access, burst read-access, or burst write-access requests. Periodic timers are also available to periodically generate user-defined refresh cycles.

The following is a list of the memory controller's main features:

- Eight memory banks
    — 32-bit address decode with mask
    — Variable block sizes (32 Kbytes to 4 Gbytes)
    — Byte parity generation/checking
    — Write-protection capability
    — Address types protection for memory bank accesses by internal masters
    — Control signal generation machine selection on a per-bank basis
    — Support for external master access to memory banks
    — Synchronous and asynchronous external masters support
- General-purpose chip-select machine (GPCM)
    — Compatible with SRAM, EPROM, FEPROM, and peripherals
    — Global (boot) chip-select available at system reset
    — Boot chip-select support for 8-, 16-, and 32-bit devices
    — Minimum two clock accesses to external device
    — Four byte write enable signals ($\overline{\text{WE}}$)
    — Output enable signal ($\overline{\text{OE}}$)
- Two user-programmable machines (UPMs)
    — Programmable-array-based machine controls external signal timing with a granularity of one quarter of an external bus clock period
    — User-specified control-signal patterns run when an internal or external synchronous master requests a single-beat or burst read or write access.
    — User-specified control-signal patterns run when an external asynchronous master requests a single-beat read or write access.
    — UPM periodic timer runs a user-specified control signal pattern to support refresh
    — User-specified control-signal patterns can be initiated by software
    — Each UPM can be defined to support DRAM devices with depths of 64, 128, 256, and 512 Kbytes, and 1, 2, 4, 8, 16, 32, 64, 128, and 256 Mbytes
    — Each UPM provides programmable timing for the following signals:

– Four byte-select lines

– Six external general-purpose lines

— Supports 8-, 16-, and 32-bit DRAM port sizes

— Glueless interface to one bank of DRAM (only external buffers are required for additional SIMM banks)

— Page mode support for successive transfers within a burst for all on-chip and external synchronous devices

— Internal address multiplexing for all on-chip bus masters supporting 64-, 128-, 256-, and 512-Kbyte, and 1-, 2-, 4-, 8-, 16-, 32-, 64-, 128-, 256-Mbyte page banks

— Glueless interface to EDO, self refresh, and synchronous DRAM devices

1.6 Communications Processor Module (CPM)

The CPM provides a flexible and integrated approach to communications-intensive environments. To reduce system frequency and save power, the CPM has its own independent RISC communications processor (CP) that is optimized for serial communications. The CP services several integrated communications channels, performing low-level protocol processing and controlling DMA.

The CPM supports multiple communications channels and protocols, and it has flexible firmware programmability. The CPM frees the core of many computational tasks in the following ways:

• By reducing the interrupt rate. The core is interrupted only upon frame reception or transmission, instead of on a per-character basis.

• By implementing some of the OSI layer-2 processing, which provides more core bandwidth for higher layer processing.

• By supporting multibuffer memory data structures that are convenient for software handling.

The CPMs are similar in the MPC850 and MPC860; both are derived from the CPM in the MC68360 QUICC; see the *MC68360 Quad Integrated Communications Controller (QUICC) User's Manual*.

The CPM's main features are as follows:

• Communications processor (CP)

— Dual-port RAM

— Internal ROM

— Two physical serial DMA (SDMA) controllers implement fourteen SDMA channels, which provide two channels each for the SCCs, SMCs, USB channel, SPI, and I^2C.

— Two independent DMA (IDMA) channels for memory-to-memory transfers or interfacing external peripherals.

— RISC timer tables

• Two full-duplex serial communications controllers (SCC2 and SCC3) that support the following:

— UART protocol (asynchronous or synchronous)

— HDLC protocol

— AppleTalk protocol

— Asynchronous HDLC protocol

— BISYNC protocol

— Transparent protocol

- — Infrared protocol (IrDA)
- — IEEE 802.3/Ethernet protocol
- — Serial ATM
- Two full-duplex serial management controllers (SMCs)
  - — UART protocol
  - — Transparent protocol
  - — GCI protocol for monitor and C/I channels (for ISDN)
- A universal serial bus (USB) controller
  - — Supports slave mode at a maximum of 12 Mbps with four USB endpoints
- Serial peripheral interface (SPI) support for master or slave modes
- Inter-integrated circuit (I^2C) bus controller
- A serial interface (SI) with a time-slot assigner (TSA) that supports multiplexing of data from SCCs and SMCs onto one time-division multiplexed (TDMa) interface
- Four independent baud rate generators (BRGs)
- Four general-purpose 16-bit timers or two 32-bit timers
- CPM interrupt controller (CPIC)
- General-purpose I/O ports

1.6.1   System Debugging and Testing Support

The MPC850 contains an advanced debug interface that provides superior debug capabilities without degrading operation speed. It supports six watchpoint pins that can be combined with eight internal comparators, four of which operate on the effective address on the address bus. The other four comparators are split—two comparators operate on the effective address on the data bus and two comparators operate on the data on the data bus. The MPC850 can compare using the =, , <, and > conditions to generate watchpoints. Each watchpoint can then generate a breakpoint that can be programmed to trigger on a programmable number of events.

The MPC850 provides a dedicated user-accessible test access port (TAP) that is fully compatible with the *IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture*. Problems associated with testing high-density circuit boards have led to development of this standard under the sponsorship of the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The MPC850 implementation supports circuit-board test strategies based on this standard.

The TAP consists of five dedicated signals, a 16-state TAP controller, and two test data registers. A boundary scan register links all device signals into a single shift register. The test logic, implemented using static logic design, operates independently of the device system logic. The MPC850 TAP implementation provides the capability to do the following:

- Perform boundary scan operations to check circuit-board electrical continuity.
- Bypass the MPC850 for a given circuit-board test by effectively reducing the boundary scan register to a single cell.
- Sample the MPC850 system signals during operation and transparently shift out the result in the boundary scan register.
- Disable the output drive to signals during circuit-board testing.

1.7 MPC850 Version Differences

Table 2 summarizes the differences that define each version of the MPC850.

Table 2. MPC850-Version Differences

Version	Functionality
MPC850	• SCC2 supports all protocols (including Ethernet) except serial ATM • SCC3 is not supported • QMC microcode for multichannel HDLC is not supported • SAR microcode is not supported • No UTOPIA interface
MPC850DE	• SCC2, SCC3 supports all protocols (including Ethernet) except serial ATM • QMC microcode for multichannel HDLC is not supported • SAR microcode is not supported • No UTOPIA interface
MPC850SR	• All functionality described in this document applies to the MPC850SR including Ethernet, ATM and multi-channel HDLC support
MPC850DSL	• SCC2 only supports Ethernet • SCC3 only supports UART • Serial ATM on an SCC is not supported • UTOPIA interface is supported • QMC microcode for multichannel HDLC is not supported • SAR microcode is supported on the UTOPIA port • I^2C is not supported

Table 3. Revision History

Revision	Date	Change
2.4	11/2001	New template format, removed references to MAC functionality, added this revision history table.

Freescale Semiconductor, Inc.

MPC850TS/D

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