ISE Design Suite 13: Release Notes Guide

UG631 (v 13.2) July 6, 2011

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/2011	13.1	Updated for the 13.1 Release. The Chapters “Download and Installation” and “Obtaining and Managing a License” have been moved to a new document titled **ISE Design Suite 13: Installation and Licensing Guide** (iil.pdf)
07/06/2011	13.2	Updated for the 13.2 Release.

Table of Contents

Chapter 3: Architecture Support and Requirements

Chapter 4: Technical Support, Services, and Documentation

XILINX®

Chapter 1

What's New in ISE Design Suite

ISE Design Suite 13.2

Highlights for this Release

Device Support

- Virtex®-7 and Kintex™-7
  - For Virtex-7 and Kintex-7, the device list has been updated with bitstream enablement
  - 7% better performance with 25% better performance for large Stacked Silicon Interconnect devices
- Virtex-7 XT and Artix™7
  - **Limited Access**

    These devices are visible but require a license to implement. Please refer the topic 7 Series Devices in Limited Access – Virtex-7 XT and Artix-7 for details.

Logic Edition

PlanAhead Enhancements

Please refer to What's New in PlanAhead Software for details.

ChipScope Enhancements

- Device configuration, programming, and debug for Kintex-7
- Serial I/O Toolkit
  - Kintex-7 GTX support for rev 1.0 silicon
  - Virtex-6 GTH support for production silicon
- Support for Digilent USB-JTAG cable plug-in
  - iMPACT, ChipScope™, SDK/XMD
  - HardWare Co-Simulation for System Generator for DSP and ISim
- ChipScope AXI Monitor in XPS
  - Implements 39 Ready/Valid handshake protocol checks
  - Added support to monitor IP with AXI3 interface

Embedded Edition

XPS Enhancements

- Enhancements to Base System Builder (BSB)
  - All user input now captured on two pages
  - Pre-production support for the Kintex-based KC705 platform
  - Support for single or dual AXI4-based MicroBlaze™ Processor designs
  - New user design setting for selection of Area or Throughput
  - When possible BSB uses a 1:1 clocking ratio for AXI4 and AXI4-Lite interfaces
- New IP Catalog option to display only AXI4 IP
- Support for simulation of external DDRx memory
- Create/Import IP wizard now supports the creation of AXI4 master, AXI4-Lite master, and AXI4-Stream IP
- Platgen performance improved through optional parallel-synthesis support when run on multi-core host machines
- Questa Advanced Simulator support
- 7 Series PLL support in Clock Wizard
- New Master/Slave Information tab in AXI4 interconnect configuration dialog

SDK Enhancements

- SDK incorporates updates from the Eclipse 3.6.2 and CDT 7.0.2 releases, providing improved stability and enhancements in this open source platform.
- Linker Script Editor: When you double click a linker script or drag/drop the file into the Editor view, the Linker Script Editor now includes Summary and Source tabs.
  - Summary tab. You can define new memory regions and change the assignment of sections to memory regions; this is useful when a memory region is divided and shared between two processors, for example.
  - Source tab. Allows you to directly edit the linker script file contents. The Generate Linker Script dialog box remains available to generate and associate linker scripts.
- Digilent Cable Support: In the Configure JTAG Settings dialog, a JTAG Cable Type set to the value "Auto Detect" can be used to detect and configure support for Digilent USB cables connected to 7 Series development boards. Also, the JTAG Cable Type "3rd Party Cable, Xilinx® Plug-in" may also be used to set cable options manually for the Digilent cable.
- MicroBlaze processor v8.20a support
- User settings in Generate Linker Script dialog saved
- Application references to the Board Support Package (BSP) and hardware projects checked

MicroBlaze Software Processor

- MicroBlaze v8.20a support
  - New version V8.20.a
    - Support for the Artix-7 family and XQ5V devices
    - Configurable use of FPGA primitives

- Up to 512 bit data width for AXI cache interconnects

Embedded IP

- Production support for XCS6-1L
- Pre-production support for the Artix-7 family and XQ5V devices
- Embedded IP Highlights
  - New AXI PCIe – supporting 6-series only (7 Series support coming in Release 13.3)
  - New AXI_QuadSPI
  - New AHB_AXI_Bridge
  - Size optimizations for AXI4-Lite interconnect in Shared Address / Shared Data mode
  - Improvements to AXI4_V6_DDRx read/write arbitration algorithm to improve throughput
  - PLBv46_PCI now supports Spartan™-6

For a list of more Embedded IP changes, please see the section Embedded IP under Important Release Information.

DSP Edition

System Generator for DSP

- Hardware Co-Simulation
  - JTAG Co-Simulation support for KC-705 board
  - Digilent Plugin support for JTAG Hardware Co-simulation (Provides 30% speed up in configuration and Co-simulation at full speed over Xilinx Platform USB)
- AXI4 Support
  - CIC Compiler v3.0 - increased input width support to 24 bits
  - Divider Generator v4.0 - increased operand width support to 64 bits
- New Features in Blocks
  - First word fall-through option in FIFO

CORE Generator and IP

- CORE Generator™ IP with Artix-7 and Virtex-7 XT Support

  Limited Access support for the Artix-7 and Virtex-7 XT device families has been added to a selection of cores in this release. These cores provide Beta support for the Artix-7 and Virtex-7 XT device families. For a comprehensive listing of IP cores supporting these new device families, click the **IP in this Release** tab at http://www.xilinx.com/ipcenter/coregen/updates_13_2.htm.
- New IP Cores
  - AXI Infrastructure IP

    These new cores make it easy to create designs using AXI4, AXI4-Lite or AXI4-stream interfaces.

- **AXI Interconnect LogiCORE IP v1.03.a** connects one or more AXI4 memory-mapped master devices to one AXI4 slave device. The AXI interconnect supports address widths from 12 to 64 bits with interface data widths of 32, 64, 128, 256, 512, or 1024 bits. Users can now implement a DDR2 or DDR3 SDRAM multi-port memory controller using MIG and AXI Interconnect IP from CORE Generator.
- **AXI Bus Functional Model (BFM) v1.9** solution, created for Xilinx by Cadence® Design Systems, enables Xilinx customers to verify and simulate communication with AXI-based IP that is being developed. The AXI BFM IP in CORE Generator delivers test-benches examples and script examples that demonstrate the use of the BFM test writing APIs for AXI3, AXI4, AXI4-Lite, and AXI4-Stream masters and slaves.
- **AXI Direct Memory Access (DMA) LogiCORE IP v4.00.a** provides a flexible interface for transferring packet data between system memory (AXI4) and AXI4-Stream target IP. The AXI DMA provides optional support of Scatter/Gather for off-loading processor management of DMA transfers and descriptor queuing for pre-fetching transfer descriptors to enable uninterrupted transfer requests by the primary DMA controllers.

- Audio, Video, and Image Processing IP
  - Video Timing Controller v3.0 now supports AXI4-Lite interface and Virtex-7, Kintex-7 device family
  - Triple Rate SDI has introduced support for Spartan®-6
- DSP Building Blocks
  - Floating-Point Operator v6.0 now supports AXI4-Stream interface, two new operators reciprocal (1/x) and reciprocal square root (1/sqrt(x)), bit accurate C-model and VHDL test bench
  - CIC Compiler v3.0 now supports AXI4-Stream interface and VHDL test bench
- Standard Bus Interfaces and I/O
  - 32-bit and 64-bit Initiator/Target for PCI now supports Virtex-7 and Kintex-7

- Additional IP supporting AXI4 Interfaces
  - The latest versions of CORE Generator IP have been updated with Production AXI4 interface support. For more detailed AXI IP support information see www.xilinx.com/ipcenter/axi4_ip.htm.
  - In general, the AXI4 interface is supported by the latest version of an IP, for Virtex-7, Kintex-7, Virtex-6 and Spartan-6 device families. Older "Production" versions of IP continue to support the legacy interface for the respective core on Virtex-6, Spartan-6, Virtex-5, Virtex-4 and Spartan-3 device families only.
  - For general information on Xilinx AXI4 support, see www.xilinx.com/ipcenter/axi4.htm.
  - A comprehensive listing of cores that have been updated in the Release 13 can be viewed at www.xilinx.com/ipcenter/coregen/updates_13_1.htm.
- PlanAhead IP Design Flow Enhancements
  - Enhancement added to inform user about availability of updated versions of IP used in their design.

Important Release Information

Documentation

The latest documentaton for Release 13 software is located at www.xilinx.com and has known changes from the Release 13 documentation on the DVD.

Known Issues

Known issues with **ISE Design Suite** can be found at the following Answer Record (AR) link: http://www.xilinx.com/support/answers/39243.htm

Known issues with **PlanAhead** software can be found at the following Answer Record (AR) link: http://www.xilinx.com/support/answers/40512.htm

Known issues with **EDK** software can be found at the following Answer Record (AR) link: http://www.xilinx.com/support/answers/39843.htm

Known issues with **System Generator for DSP** software can be found at the following Answer Record (AR) link: http://www.xilinx.com/support/answers/29595.htm

Device Support

7 Series Devices in Public Access - Virtex-7 T and Kintex-7

- Bitstream generation has been enabled for this release
- Changes will be made to the Kintex-7 and Virtex-7 7 Series FPGA Transceiver Wizard in a future
- Xilinx software release. This change will require that the 7 Series FPGA Transceiver Wizard be rerun to utilize the latest capabilities
- 7% better performance with 25% better performance for large Stacked Silicon Interconnect devices
- Speed files, Power, and Packages are in ADVANCED status. Refer to the Virtex-7/Kintex-7 FPGA Data Sheet: DC and Switching Characteristics for a detailed explanation on the different status.
- The following devices have been **removed** from the ISE Design Suite 13.2 software
  - **Virtex-7T**
    - xc7v285t
    - xc7v450t
    - xc7v855t
  - **Kintex-7**
    - xc7k30t
- The following packages have been **removed** from the ISE Design Suite 13.2 software
  - **Virtex-7T**
    - xc7v1500t (fhg1157 & ffg1761)
    - xc7v2000t (ffg1925)
  - **Virtex7-XT**
    - xc7vx485t (ffg1929)
  - **Kintex-7**

  - xc7k70t (sbg324)
- Beginning with ISE Design Suite 13.2, Xilinx requires users to select all `IOSTANDARDs` and pin placement in their design prior to generating a bitstream. Please see Xilinx Answer Record 41615 for more information

Note: For additional Known Issues, please see Xilinx Answer Record 40905.

7 Series Devices in Limited Access – Virtex-7 XT and Artix-7

In this release, the following devices are Limited Access and are license controlled:

- Xilinx Virtex-7 XT
- Xilinx Artix-7

Limited Access devices are currently Beta-level quality and access requires a device-specific license. Contact your Sales Representative for more information about obtaining the required license.

Table 1-1 provides information on which Artix-7 software features are not fully supported (noted limitations or license required).

Table 1-1: **Artix-7 Software Features Not Fully Supported**

Feature	Supported in Limited Access	Device-Specific License Required
Synthesis - 3rd party	Yes (Refer to the section Synthesis-3rd Party)	No
IP Support	Yes (Refer to the section IP Support)	No
All Devices Available	Limited (A8/A15 support in Release 13.3)	Yes
Implementation Tools	Yes	Yes
7 Series Transceiver Wizard	No	N/A
Design Preservation and Team Design	No	N/A
Partial Reconfiguration	No	N/A
ChipScope	No	N/A
SSO and SSN	No	N/A
Bitstream Generation	No	N/A

Table 1-2 provides information on which Virtex-7 XT software features are not fully supported (noted limitations or license required).

Table 1-2: **Virtex-7XT Software Features Not Fully Supported**

Feature	Supported in Limited Access	Device-Specific License Required
Synthesis - 3rd party	Yes (Refer to the section Synthesis-3rd Party)	No
Simulation - 3rd Party	Limited (Mentor Graphics ModelSim/QuestaSim only)	No
IP Support	Yes (Refer to the section IP Support)	No
All Devices Available	Yes	Yes
Implementation Tools	Yes	Yes
7 Series Transceiver Wizard	Yes (Refer to the section 7 Series FPGA Transceiver Wizard)	N/A
Design Preservation and Team Design	No	N/A
Partial Reconfiguration	No	N/A
ChipScope	No	N/A
SSO and SSN	No	N/A
Bitstream Generation	No	N/A

Synthesis-3rd Party

Synplify® Pro - Please contact your Synopsys Technical Support for more information on the version supporting limited access devices

Precision® RTL - See Xilinx Answer Record 42813 for more information.

IP Support

For detailed information on IP support, refer to the IP Release Notes Guide.

Known Issues for Device Support

Artix-7

Details: Incomplete Package support for the XC7A30T devices in PlanAhead. PlanAhead does not support the following packages for 7A30T devices

- xc7a30t-csg324-1
- xc7a30t-csg324-2
- xc7a30t-csg324-3

Resolution: The workaround is to use do pin-planning via the UCF file, instead of PlanAhead software for this device.

GTP SecureIP model

Details: This release does not have support for the GTP E2 SecureIP simulation model.

Resolution: This will be supported in the next release.

Incomplete Package support

Details: Not all devices have package files in this release.

Resolution: This will be supported in the next release.

7 Series FPGA Transceiver Wizard

Details: Currently the generation of the GTHE2 is not supported.

Resolution: Please contact Xilinx Technical Support for more information.

Note: For additional Known Issues, please see Xilinx Answer Record 40905.

XPS

- Base System Builder support is in Pre-Production status for the KC705 board and all 7 Series designs targeting custom boards. Several embedded IPs supported by the KC705 are not yet available, and timing closure and design functionality is not guaranteed.

Embedded IP

- New Embedded IP Cores (v1.00.a)
  - AXI Interconnect Generator
  - AXI_PCIE
  - Cadence AXI BFM Wrappers – AXI3 and AXI4 Master/Slave Streaming
  - AXI_Master_Burst_IPIF
  - AXI_QuadSPI
  - AHB_AXI_Bridge
- Existing Embedded IP Updates – see individual IP change logs for individual enhancements and CRs fixed
  - AXI Interconnect – v1.03.a
  - AXI-4 Stream CIP Wizard Example
  - AXI V6 MIG DDRx – v1.03.a
  - AXI 7-series DDRx – v1.01.a
  - MPMC – v6.04.a
  - Proc_common – v3.00.a
  - PLBv46_pci – v1.04.a
  - Support for S6
  - PLBv46_pcie – v4.07.a
  - AXI_BRAM_Cntrl – v1.03.a
  - AXI_Datamover – v2.01.a
  - AXI_SG – v2.02.a
  - AXI_DMA – v4.00.a
  - AXI_CDMA – v3.01.a
  - AXI_VDMA – v3.01.a
  - COREGen AXI VDMA – v3.01.a

  - AXI_Ethernet – v3.00.a
  - AXI_FIFO_MM_S – v2.01.a
  - ChipScope AXI Monitor – v3.00.a
  - AXI_Timer – v1.02.a
  - AXI GPIO – v1.01.a
  - XPS UARTLite – v1.02.a
- Improvements to AXI4_V6_DDRx read/write arbitration algorithm to improve throughput
- Size optimizations for AXI4-Lite interconnect in Shared Address / Shared Data mode

System Generator for DSP

New Constraints File Requirement for Generating a 7 Series Device Bitstream

If you are using the System Generator for DSP bitstream compilation target flow and also target a 7 Series device (Artix-7, Kintex-7, Virtex-7), you may run into a Bitgen error if you have not included a constraints file that specifies `LOC` and `IOSTANDARD` constraints for all pins. This change in behavior is documented in Xilinx Answer Record 41615. For workarounds specific to System Generator for DSP, refer to Xilinx Answer Record 42911.

ISE Design Suite 13.1

Highlights for this Release

ISE Design Suite

- Team Design
- Up to 100 times simulation acceleration via ISim Hardware Co-simulation
- AXI4 tool and IP support is now "Production" status
- Plug-and-Play IP Initiative
  - CORE Generator™ 2.0 introduction
  - IEEE P1735 Version 1 decryption interoperability
- Windows 7 Professional support

Device Support

Xilinx introduces the following device support for the 13.1 release:

- Kintex™-7
- Virtex®-7 (Including 7VX485T)

Logic Edition

The following describes what's new in Logic Design Tools in ISE 13.1.

Project Navigator

- Embedded Development Kit (EDK) Integration Improvements
  - Support for multiple ELF files and automatic detection of ELF files referenced by EDK designs
  - Ability to control associations between ELF files and specific processors defined in XMP files
  - Ability to select an Evaluation Development Board in the New Project Wizard, New Project dialog box, or Design Properties dialog box
  - Ability to export hardware design before running implementation
  - Ability to automatically launch the Software Development Kit (SDK) when exporting a design
- Compare Projects feature includes additional categories and layout improvements
- SmartXplorer now features support for power-dedicated and custom strategies
- CORE Generator™ has the ability to update a core to the latest version as well as the ability to check all core versions
- Ability to create a new System Generator source in Project Navigator
- Ability to create a new System Generator source in Project Navigator
- Support for viewing TWR reports in Timing Analyzer

FPGA Editor

- New Lock Layers toolbar button, which locks the current layer visibility settings for all zoom levels.

iMPACT

- New SPI/BPI programming support:
  - Numonyx P30 bottom boot is supported, in addition to top boot.
  - Winbond W25Q is supported up to 128Mb.
  - Winbond W25Q support for the CV revision has been added.

ChipScope Pro

- ChipScope Pro HDL (VHDL and Verilog) Debug probe using PlanAhead and XST Synthesis flow
  - Enable users to mark debug nets on HDL or XCF constraint file
  - When MARK_DEBUG attribute is used:
    - Nets are preserved (not optimized away)
    - Nets appear in the ChipScope view in the PlanAhead view so users can assign to debug cores
- ChipScope Pro HDL Debug probe using PlanAhead and Synplify Synthesis flow
  - Enable users to mark debug nets on HDL (VHDL and Verilog) or SDC
  - When MARK_DEBUG attribute is used:
    - Nets are preserved (not optimized away)
    - Nets appear in the ChipScope view in the PlanAhead view so users can assign to debug cores
- BERT for Virtex®-6 GTX and GTH available in PlanAhead and ChipScope Flow
  - Also added low- and mid-range line rate support for IBERT V6 GTH
- Startup Trigger Mode
  - Using Project Navigator, Core Inserter, and Analyzer Tools
  - Using PlanAhead software and Analyzer Tools
- BERT sweep test plot GUI
  - Built-in graphical viewer of IBERT sweep test results for Virtex®-6 GTX/GTH FPGA transceivers
  - Standalone graphical viewer for offline analysis of IBERT sweep test results for Virtex®-6 FPGA GTX/GTH, Spartan®-6 FPGA GTP, and Virtex®-5 FPGA GTX transceivers
- Tutorials:
  - PlanAhead Tutorial: Debugging with ChipScope Analysis
  - ChipScope IBERT: Basic IBERT design flow

ISE Simulator

- Supports simulation of AXI BFM
- Relaunch of simulation from the ISIM GUI

Embedded Edition

The following describes what's new in Embedded Tools and IP in ISE Design Suite 13.1.

EDK Overall Enhancements

- Consistent SDK workspace selection behavior across Project Navigator, Xilinx Platform Studio (XPS), and SDK.
- TDP device-based licensing support.

XPS Enhancements

- Changes to Base System Builder
  - AXI systems are now the default in Base System Builder for Spartan®-6, Virtex®-6, and 7 Series designs. Base System Builder only supports AXI systems for 7 Series designs.
  - New shared bus interconnect used for low frequency peripheral bus, reduces design size.
- Changes to System Assembly View (SAV)
  - New DRC feature allows you to run design rule checks at any time.
  - When AXI IP is added in SAV, the following functions are automatically completed: bus, clock, and reset connections, and address generation
  - When adding an AXI MicroBlaze processor instance, the following functions are automatically completed: interconnect, DRAM memory and cache connections, debug connections, clocks, and LMB BRAM
  - You can now modify the order of IP listed in the SAV
  - For multi-processor systems, you can filter on processor system instance in the SAV
- Other XPS Changes
  - All software development tools have been removed from XPS
  - Software projects have been removed from XPS
  - The main toolbar has been streamlined and now contains fewer buttons.
  - Create and Import IP (CIP) wizard now supports creation of AXI4 and AXI4-Lite slave peripherals
  - AXI BFMs project generation now included in CIP wizard. **Note**: A license for AXI BFMs must be purchased separately.
  - ELF files can now be assigned for implementation or simulation and remain synchronized with Project Navigator.
  - Debug Wizard supports inclusion of AXI monitors and hardware/software co-debug of AXI-based designs.
  - When the XPS design is a submodule in a Project Navigator project, simulation is only available in Project Navigator.
  - When you export your design to SDK, the SDK workspace is no longer set automatically.

SDK Enhancements

- Updated to Eclipse 3.6 and CDT 7.0 Helios release.
  - Updated functionality and improved stability while retaining the familiar user interface
  - Capture console log to files.
- Cygwin no longer required or shipped
  - GNU Tool Chain for MicroBlaze and PowerPC built natively without Cygwin
  - GnuWin32 utilities provided for common UNIX/Linux functions
- Usability Updates
  - ELF-only debugging
  - Launch management
  - Flow checking, including BSP deletions and hardware change detection.
  - User assistance, including hints, context sensitive help and preference settings.
  - Software repository information saved to minimize setup when using revision control.
  - Automation for Flash read-only region behaviors.
- 7 Series initial support in XMD
- TDP device-based licensing support

Project Navigator/EDK Integration Enhancements

- Recognition of multiple processor instances in .xmp.
  - Previous versions assumed a single processor
  - Ability to control associations between ELF files and specific processors defined in XMP files.
- Separate .elf sources for implementation and simulation.
  - elf files now assigned per processor instance.
  - Automatic detection of ELF files referenced by EDK designs.
- New “Export Hardware Design to SDK without Bitstream” process allows you the ability to export hardware design before running implementation.
- Ability to automatically launch the Software Development Kit (SDK) after design export (optional).
  - SDK workspace handling consistent with XPS and standalone SDK.
- Ability to select an Evaluation Development Board in Project Navigator’s New Project Wizard, New Project dialog box, or Design Properties dialog box.

MicroBlaze Soft Processor

- New version V8.10.a
- Support for 7 Series Kintex and Virtex devices
- AXI now the default interface for 7 Series designs
- MicroBlaze Configuration wizard support Fault Tolerant features
- Added Error Correction Code (ECC) to LMB BRAM memory connected to MicroBlaze
- Added parity protection on MicroBlaze cache and MMU memory

- New instructions added
  - Count Leading Zeros (CLZ)
  - Memory Barrier (MBAR)
- Stack overflow and underflow detection
- New parameter allows AXI4-Stream / FSL instructions in user mode

Embedded IP

- New Embedded IP
  - AXI 7-Series DDRx
  - AXI External Peripheral Controller
  - AXI to AHBLite Bridge
  - AXI Master Lite IP Interface (IPIF)
- Embedded IP now available in CORE Generator
  - CORE Generator AXI VDMA

DSP Edition

The following describes what's new in System Generator for DSP and DSP IP in ISE 13.1.

System Generator for DSP

- Support for MATLAB/Simulink 2011a.
- All System Generator blocks now support Kintex-7 and Virtex-7 devices.
- New blocks
  - 7 Series DSP48E1, Complex Multiply 5.0, DSP48 Macro 2.1, FIR Compiler 6.2, VDMA Interface 3.0.
- System Generator support for AXI PCore and HW Co-simulation.
- New context menus speed adding and connecting blocks (Beta). For details on this feature, see Chapter 5 of the System Generator for DSP Reference Guide.
- Choice to have tools automatic create a Hardware Interface Document. For more details on this feature, see the System Generator token topic in the System Generator for DSP Reference Guide.
- System Generator IP
  - Floating-point Operator, CORDIC, Divider Generator, CIC Compiler, DSP48 Macro, Multiply-Add, and Multiply-Accumulate.

CORE Generator and IP

The following describes what's new in CORE Generator™ software and IP cores:

Introducing CORE Generator IP with Virtex®-7 and Kintex™-7 support

New IP Cores

- Audio, Video and Image Processing IP
  - Object Segmentation v1.0 (AXI4-Lite)
    - Used in conjunction with the Image Characterization LogiCORE IP to convert statistical data provided into a list of objects that meet a user-defined set of object characteristics.

    - AXI Video Direct Memory Access v1.0 (AXI4, AXI4-Stream, AXI4-Lite)
        - Provides a flexible interface for controlling and synchronizing video frame stores from external memory. Multiple VDMAs from different clock domains can be linked together to control frame store reads and writes from multiple sources.
- Communication DSP Building Blocks
    - Linear Algebra Toolkit v1.0 (AXI4-Stream)
        - Implements basic Matrix operations - Matrix-Matrix Addition, Subtraction, Matrix-Scalar Multiplication and Matrix-Matrix Multiplication.
        - This IP provides flexible and optimized building blocks for developing complex composite functions for various signal and data processing applications.
- FPGA Features and Support
    - 7 Series FPGA Transceivers Wizard v1.3
        - Configures one or more Virtex-7 and Kintex-7 FPGA GTX transceivers either from scratch, or using industry standard templates, using a custom Verilog or VHDL wrapper.
        - Also provides an example design, testbench, and scripts to allow you to observe the transceivers operating in simulation and in hardware.
    - XADC Wizard v1.2
        - The XADC Wizard generates an HDL wrapper to configure a single 7 Series FPGA XADC primitive for user-specified channels and alarms.
- Standard Bus Interfaces and I/O
    - 7-Series Integrated Block for PCI Express (PCIe) v1.0 (AXI4-Stream)
        - Implements 1-lane, 2-lane, 4-lane, or 8-lane configurations. The IP uses the 7 Series Integrated Hard IP Block for PCI Express in conjunction with flexible architectural features to implement a PCI Express Base Specification v2.1 compliant PCI Express Endpoint or Root Port.
        - Unique features of the LogiCORE IP for PCI Express are the high performance AXI Interface, optimal buffering for high bandwidth applications, and BAR checking and filtering.
- Wireless IP
    - Triple Rate SDI v1.0 (AXI4-Stream)
        - Provides receiver and transmitter interfaces for the SMPTE SD-SDI, HD-SDI, and 3G-SDI standards.
        - The Triple-Rate SDI receiver and transmitter are provided as unencrypted source code in both Verilog and VHDL, allowing you to fully customize these interfaces as required by your specific applications.
    - 3GPP LTE PUCCH Receiver v1.0 (AXI4-Stream)
        - Provides designers with an LTE Physical Uplink Control Channel Receiver block for the 3GPP TS 36.211 v9.0.0 Physical Channels and Modulation (Release 9) specification.
        - Support for channel estimation, demodulation and decoding.

Additional IP supporting AXI4 Interfaces

- The latest versions of CORE Generator IP have been updated with Production AXI4 interface support. For more detailed support information see www.xilinx.com/ipcenter/axi4_ip.htm.
- In general, the AXI4 interface will be supported by the latest version of an IP, for Virtex®-7, Kintex™-7, Virtex®-6 and Spartan®-6 device families. Older "Production" versions of IP will continue to support the legacy interface for the respective core on Virtex®-6, Spartan®-6, Virtex®-5, Virtex®-4 and Spartan®-3 device families only.
- For general information on Xilinx AXI4 support see www.xilinx.com/ipcenter/axi4.htm.
- A comprehensive listing of cores that have been updated in this release can be viewed at www.xilinx.com/ipcenter/coregen/updates_13_1.htm.

CORE Generator Enhancements

- Introducing support for IP-XACT based IP repositories for Xilinx and Alliance Program Member IP. (Requires no changes to existing CORE Generator, PlanAhead and Project Navigator user flows.)
- Addition of "Manage IP" pull-down menu to provide repository and IP management features.
- Display of AXI4 support by each IP in the IP catalog has been expanded to display the various AXI4 interfaces in separate sortable columns: AXI4, AXI4-Stream and AXI4-Lite
- Individual ports in IP symbols can now be grouped into AXI4 channels for simplified symbol views.

PlanAhead IP Design Flow Enhancements

- Introducing support for IP-XACT based IP repositories for Xilinx and Alliance Program Member IP (Requires no changes to the existing PlanAhead software IP flow).
- Display of AXI4 support by each IP in the IP catalog has been expanded to display the various AXI4 interfaces in separate sortable columns: AXI4, AXI4-Stream, and AXI4-Lite.
- Support added for Automatic IP Upgrade flow.

Important Release Information

General

- Pinouts on Kintex-7 and Virtex-7 devices are subject to change because package files are not yet finalized for these families. Pinout changes may require design re-implementation in a future Xilinx software release.
- Default IO standards for Kintex-7 and Virtex-7 devices will change in a future Xilinx software release.
- Changes will be made to XC7V1500T and XC7V2000T device models in a future Xilinx software release. 13.1 implementation design files (.NCD) targeting these devices will be invalidated at that time, and designs will need to be re-implemented.

- Changes will be made to the Kintex-7 and Virtex-7 GTX component models in a future Xilinx software release. This change will require that the 7 Series FPGA Transceivers Wizard be rerun for each instance.
- IBIS and HSPICE models are not yet available for Kintex-7 and Virtex-7 devices.

Known Issues

Known issues with **ISE Design Suite** can be found at the following Answer Record (AR) link: http://www.xilinx.com/support/answers/39243.htm

Known issues with **PlanAhead** can be found at the following Answer Record (AR) link: http://www.xilinx.com/support/answers/40512.htm

Known issues with **EDK** can be found at the following Answer Record (AR) link: http://www.xilinx.com/support/answers/39843.htm

Known issues with **System Generator for DSP** can be found at the following Answer Record (AR) link: http://www.xilinx.com/support/answers/29595.htm

ISE Simulator

- Recompile and Relaunch simulation
  - You can now edit files, re-compile, and re-launch a simulation within the ISE Simulation GUI
- Full Access to Hardware Co-Simulation
  - The limited customer access restrictions have been removed.
  - An additional license is no longer required.
- Design Environment Integration
  - You can now launch ISim from PlanAhead and Project Navigator.
- ISim User Guide Improvements
  - There is a new section on Hardware Co-Simulation.
  - The Tcl Commands chapter has been re-organized.

XPS

- All software development tools have been removed from XPS.
- AXI based MicroBlaze designs are always built using instruction and data caches.
- The main toolbar has been streamlined and now contains fewer buttons.
- Create and Import IP (CIP) wizard now supports creation of AXI4 and AXI4-Lite slave peripherals.
- AXI BFMs project generation now included in CIP wizard.
- ELF files can now be assigned for implementation or simulation and remain synchronized with Project Navigator.
- Debug Wizard supports inclusion of AXI monitors and hardware/software co-debug of AXI-based designs.
- When the XPS design is a submodule in a Project Navigator project, simulation is only available in Project Navigator.
- When you export your design to SDK, the SDK workspace is no longer set automatically set.

SDK

- Cygwin no longer required:
  - Custom makefiles use Windows style paths
  - xbash removed
- MicroBlaze v8.10a support
- XMDStub support removed

Project Navigator/EDK Integration

- Project Navigator will no longer support xmp as the top-level source.
- New messaging to add top-level HDL results in consistent constraint handling.

Embedded IP

- Several Existing core updates
  - See individual change logs and datasheets for specifics.
- AXI Enhancements
  - AXI BRAM Controller – Microblaze ECC Block RAM support.
  - AXI Interconnect – Shared Bus Mode.
  - Partitioned Clock Domains – AXI VDMA, AXI CDMA, AXI DMA.
  - AXI Ethernet – Full checksum offload.

System Generator for DSP

VHDL Library Support for Black Box Import

This new Black Box feature allows you to import VHDL modules that have predefined library dependencies. For example, similar but independent sub-modules can now be compiled into different libraries other than "work". A detailed example of how to use this new feature can be found in the online Help topic titled "Black Box VHDL Library Support".

Performance Improvements

- Support for fast simulation model for AXI FFT that provides a 42x speed up.
- 33% improvement in 1st-time initialization of a model.
- 2-3x improvement in simulation speed.

MATLAB Support

- MATLAB 2010a and 2010b are fully supported.
- Beta support is provided for MATLAB 2011a.
- MATLAB must be installed in a directory with no spaces (e.g., C:\MATLAB\R2010b).
- The Fixed-Point Toolbox is required if a Gateway Out block has an output greater than 53 bits. Signals internal to the Xilinx Gateway In and Gateway Out blocks can be larger than 53 bits without needing the Fixed-Point Toolbox.
- For Linux, MATLAB 2010a requires the Red Hat Enterprise Desktop 5.2, 32-bit/64-bit Operating System. It does not work with Red Hat Enterprise Linux WS v4.7.

New Blocks

Complex Multiply 5.0

This block is based on the Xilinx® LogiCORE™ IP Complex Multiplier that implements AXI4-Stream compliant, high performance, optimized complex multipliers based on user-specified options.

DSP48 Macro 2.1

The Xilinx LogiCORE™ DSP48 Macro provides an easy-to-use interface that abstracts the XtremeDSP™ slice and simplifies its dynamic operation by enabling the specification of multiple operations via a set of user-defined arithmetic expressions. New in this version of the core is the ability to control resets and clock enables of the registers within the XtremeDSP Slice.

DSP48E1

The Xilinx DSP48E1 block is an efficient building block for DSP applications that use Xilinx Virtex®-6 devices. The DSP48E1 block provides access to the pre-added and control of the registers within the silicon.

FIR Compiler 6.2

This block is based on the Xilinx® LogiCORE™ IP FIR Compiler v6.2 that implements AXI4-Stream compliant, high performance, optimized complex multipliers based on user-specified options.

VDMA Interface 3.0 (Beta)

This block is based on the AXI Video Direct Memory Access (AXI VDMA) core which is a soft Xilinx IP core providing high-bandwidth direct memory access between external DDR memory and the AXI4-Stream interface. Initialization, status, and management registers are accessed through an AXI4-Lite slave interface which can be configured using an MCode block. A MATLAB utility function is provided to generate the necessary logic to easily connect your System Generator design to external DDR memory.

Previous Versions of System Generator for DSP Release Notes

Previous versions of System Generator for DSP release notes are located in Chapter 3 of the **System Generator for DSP Getting Started Guide (v 12.4)**. This getting started guide is located online at the following URL:

http://www.xilinx.com/support/documentation/dt_sysgendsp_sysgen12-4.htm

XILINX®

Chapter 2

What's New in PlanAhead Software

PlanAhead Software 13.2

GUI and Project Improvements

Clock Domain Interaction Report

The PlanAhead™ software 13.2 has added the capability to analyze timing paths that cross between clock domains defined in UCF as PERIOD constraints. The Clock Domain Interaction report is based on the static timing analysis estimation engine that is available in PlanAhead, and is not provided by the signoff TRACE timing tool. The PlanAhead timing analysis engine builds a matrix of all possible combinations that can exist between clock constraints and detects if there are paths between them. There is a graphical report with a color coded table that indicates whether paths were found, and whether they were properly constrained, partially constrained, or unconstrained. There is also an ASCII version of the report. The report can be generated by selecting **Tools > Timing > Report Clock Interaction** or by invoking the `report_clock_interaction` Tcl command.

Invoke TRACE After Implementation

The PlanAhead software has added the ability to call TRACE without re-running the entire implementation flow. In prior releases, if you wanted to re-run TRACE to generate a TWR or TWX timing report file with different options than those set in the run strategy, you would have to either re-run the entire implementation run or manually go to the run directory and invoke TRACE with the new options you wish to use. The PlanAhead software has added a shortcut in the Graphical User Interface (GUI) to run TRACE with different options on a post-implementation design.

Global Include Files

Verilog support for RTL development in the PlanAhead software now includes support for global include files similar to that of Project Navigator.

Tool Tip Localization

The GUI tool tips now include Chinese and Japanese language versions of all the text in the tool tips. These can be enabled in **Tools > Options > General** under the **Language & Tooltips** section.

Schematic View Default for Opened RTL Design

When the RTL design is opened, the default layout view now opens to the schematic view.

New Clock Planning View Layout

There is a new Clock Planning view layout to facilitate the planning and placement of clock resources in the design. The Clock Planning view layout is available from the Layout menu or from the pulldown Layout Selector in the toolbar menu.

Save Workspace View with Custom Layout Save

In customized GUI layouts, the PlanAhead software also saves changes to the Workspace view layout, such as the Device view and Project Summary, along with other user-defined layout changes.

Hierarchical Design Methodology Support

The PlanAhead software has added the ability to configure partition settings in both the synthesis and implementation run settings dialogs. This allows the ability to control partition behavior directly in the run settings section of the tool. Once a partition has been selected in the RTL or Netlist views, there is a new option in the Flow Navigator to control the partition settings for both synthesis and implementation.

Pin Planning Features

Initial 7 Series SSN Report

Support for Simultaneous Switching Noise (SSN) signal integrity checks and recommendations have been added for certain 7 series devices. This report will likely be enhanced based on further characterization in the future. Unsupported devices are indicated when running the report, using either the **Tools > Run Noise Analysis** command or the equivalent Tcl command.

7 Series HP/HR Bank Support

The PlanAhead software supports HP and HR Bank visualization for 7 series devices in the Device and Package views.

Automatically Sort Package Pins View

After setting the Device Configuration Mode, the PlanAhead software offers the option to automatically sort the Package Pins view by the Config column so newly configured pins are listed first.

Export IBIS Model Command Removed

IBIS model generation is not supported in the PlanAhead software. PlanAhead 13.1 provided a Tcl command and a menu command to export an IBIS model configured for your device, which issued a warning message stating that this capability was not supported. This menu option and Tcl command have been removed until the feature is fully supported. The standalone IBISWriter tool supports IBIS model generation for Spartan®-6, Virtex®-6 and 7 series devices. Refer to the *Command Line Tools Users Guide (UG628)* for more information on using the IBISWriter.

Improved Tcl Online Help and Documentation

Additional details have been added to Tcl command reference documentation, available in the *PlanAhead Software Tcl Command Reference Guide (UG789)* (http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_2/ug789_tcl_commands.pdf), and the online help text available through the Tcl `help` command.

PlanAhead Software 13.1

This section provides an overview of the PlanAhead software 13.1 release. See the related chapters in the PlanAhead User Guide (UG632), for more information.

ISE Simulator Integration

The PlanAhead software has integrated the Xilinx ISE Simulator (ISim) into the design flow. This new integration enables development and verification of designs completely within the PlanAhead user interface. PlanAhead now has support for simulation-only sources added to the project, which is performed either in the new project wizard or in the add sources dialog. The Flow Navigator provides access to ISE Simulator.

You can invoke ISim:

- After RTL Design for behavioral simulation
- After Implementation for timing simulation

Hierarchical Design Methodology Support

The PlanAhead software supports the Hierarchical Design features as described in the following subsections.

- Incremental XST flow in RTL projects
- Importing a partition into a different hierarchy than the one in which the partition was created
- AREA_GROUPS within partitions
- Black box support in Synthesis and Implementation
- Boundary optimization for constants and unconnected inputs and outputs on partition ports
- Defining partitions for Design Preservation in Netlist-based projects

Team-Based Design Support

PlanAhead 13 adds support for new team-based design methodology. Team-based design supports multiple engineers implementing at a module level within a design to work in parallel. The flow then supports assembling the module-level runs by a team leader at the top level with support for preservation levels to control the placement and routing information that is kept during import.

See the *Hierarchical Design Methodology Guide (UG748)* and Chapter 13, Hierarchical Design Techniques, in the *PlanAhead User Guide (UG632)* for more information.

Design Preservation RTL Support

PlanAhead 13 enhances support for design preservation flows by adding incremental compilation for RTL synthesis of partitions with XST. The design preservation flow allows a designer to mark portions of a design to be preserved in subsequent iterations and enabled incremental compilation. In prior releases, design preservation was only supported post synthesis. RTL-level control was added to provide designers an easier to use flow to control partitions throughout the design flow from synthesis through implementation within the PlanAhead user interface.

See the *Hierarchical Design Methodology Guide (UG748)* and Chapter 13, Hierarchical Design Techniques, in the *PlanAhead User Guide (UG632)* for more information.

Partial Reconfiguration Support

PlanAhead provides an interface to Partial Reconfiguration with appropriate licensing.

See the *Partial Reconfiguration User Guide (UG702)* for more information.

Project Navigator Project File (.xise) Support

The New Project wizard lets you specify an ISE project file without requiring the specification of all project sources. The PlanAhead software:

- Parses the XISE project file
- Adds RTL and simulation sources, including CORE Generator™ software cores and Block Memory Model (BMM) file

PlanAhead can now also determine relevant run options for Synthesis and Implementation tools and can configure the default run to match based on settings in the XISE project file.

New and Modified Project Management Features

The following subsections describe the new and modified features in PlanAhead projects. In PlanAhead 13, you can:

- Import sources from Project Navigator
- Order source files automatically or manually for proper compilation by XST
- Discover the top-module name automatically
- Support 'include statements inside HDL more robustly
- Support Xilinx Synthesis Technology (XST) XCF constraint files
- Identify unused source files
- Launch Runs without copying sources to the Run directory
- Archive projects
- Customize the Text Editor font

Graphical User Interface Enhancements

The PlanAhead software for release 13 has further enhanced the "layered complexity" of the Graphical User Interface (GUI) to provide an intuitive environment for both new and advanced users.

The left-side panel of the interface is a "Flow Navigator," which exposes a push-button flow from Project Management, through RTL Design, Netlist Design, Implemented Design, to Device Programming and Debugging. The new integration with ISim provides timing and behavioral simulation, which are exposed where appropriate for use in the Flow Navigator menu options. A new information window and an enhanced Tcl Console and Messaging window are also available.

The following subsections describe the new features and enhancements in the PlanAhead software release in the ISE® Design Suite.

Main Menu Enhancements

Workspace Views

The PlanAhead workspace views are redesigned with an auto-fit selection. A dropdown in the main toolbar lets you select applicable views for the open Project. The workspace views now contain dock/undock, float, minimize/maximize, and restore buttons.

Search Option

PlanAhead has added a search text box on the main menu to search through all the menu options for the specified text.

Export Options

A new option in the PlanAhead File > Export > Export IBIS Model is available for an open design. The Input/Output Buffer Information Specification (IBIS) is used analyze the design. The IBIS model exported from PlanAhead is compliant with the IBIS version 4.2, and uses the defaults of that specification.

Single Click Implementation

PlanAhead now allows you to click on the Implementation button in the Flow Navigator, and the tool will launch a dialog box prompting you to launch synthesis first if you have an RTL project and the synthesis run is out of date. This "single-click" implementation of RTL requires that you have PlanAhead in GUI mode. If you launch synthesis first and then close the project, only the currently running Synthesis run completes and the Implementation run does not launch.

Source View Enhancements

The PlanAhead release 13 provides enhanced views for source file structures and editing.

Third-Party Text Editor Support

PlanAhead now allows the ability to use third-party editors for editing source code files.

Message Manager

A new Messages view consolidates error, critical warning, warning, and informational messages from PlanAhead and ISE software tools into a single view. Messages are linked to the source code to allow for quick exploration and resolution of any errors or warnings.

Netlist View Additions and Modifications

The following subsections describe the additions and modifications to the PlanAhead Netlist view.

Clocking Resource View

The new Clocking Resource view enables you to visualize and assign clocking-related sites and physical resources within the FPGA.

Folders for Component Switching Limits

There are new folders in the Timing Results view imported from TRACE that better organize the component pin switching limit violations with setup and hold violations. The violations are sorted and the worst violation is displayed first within a constraint.

Enhanced Slack Histogram Report

PlanAhead release 13 contains an improved slack histogram feature which creates a graphical bar chart corresponding to collections of paths within ranges from most negative to most positive.

Device View Enhancements

PlanAhead Release 13 contains the following enhancements.

Device Resource Details

The Device view in PlanAhead has been enhanced to provide more detail for device resources, such as pins on slices and BEL-level pins for Virtex®-6 and Virtex-7 devices, and the Timing Path provides annotation on pins upon full placement.

Multiple Instance Drag and Drop

PlanAhead now allows moving multiple instances in the device view at the same time. This allows users to move instances that are already placed in a group, and all location constraints are translated together.

Schematic View Enhancements

PlanAhead supports tracing logic between two selected objects in the Schematic view. Any two objects can be selected, and the PlanAhead software will trace and draw any intermediate logic connections between them within a schematic.

XPA Integration

PlanAhead has added the ability to launch Xilinx Power Analyzer (XPA) to analyze power on implemented designs. To launch XPA, open an implemented design, and click the XPower Analyzer icon.

RTL Design Additions and Modifications

Text Editor Options

PlanAhead release 13 allows for customization of fonts for comments, and keywords, supports integration of third-party text editors, and allows for easier use of Xilinx Language Templates. See PlanAhead User Guide (UG632), Chapter 5, RTL Design.

IP Catalog

The PlanAhead release 13 enhancements in the IP Catalog are:

- The CORE Generator™ software IP catalog now supports migration of older superseded cores to the currently supported version.
- PlanAhead now supports canceling IP generation tasks that block other operations in the GUI.

Source File Exploration

PlanAhead can determine the top module in an RTL design automatically, or give you the ability to define it manually.

You can reorder source files, either automatically or manually, for compilation and synthesis, and automatically or manually enable or disable RTL source files as required by the top-level module.

Power Estimation Enhancements

PlanAhead release 13 has Power Estimation available on Virtex-5, Virtex-6, and Spartan®-6 device families.

Partitions Control

PlanAhead release 13 provides control of partitions at the RTL level in synthesis with XST.

Additional ChipScope Features

The PlanAhead software release 13 added the ability within the ChipScope™ Pro Debug Analyzer to tag RTL nets using a new HDL Debug Probe feature that supports the following HDL debug flows:

- PlanAhead and Xilinx Synthesis Technology (XST).
- PlanAhead and Synplify and Synplify Pro from Synopsys, Inc.
- PlanAhead and Precision RTL Synthesis from Mentor Graphics, Inc.

See Chapter 12, Programming and Debugging the Design, in the PlanAhead User Guide (UG632).

Pin Planning Changes

The following subsections describe the PlanAhead 13 changes to the pin planning features.

Package View Legend and Spreadsheet Manipulation

A new legend to the Device and Package view allows you to view or hide specific layers and objects, and provides a legend for layer colors and pin shapes.

The spreadsheet-like Package Pins view can be edited, sorted, flattened, and filtered for better visibility on multifunction pins.

Alternate Part Definition

PlanAhead release 13 has the ability to define alternative parts to a design (for Virtex-5, Virtex-6, and Spartan-6 devices only). Some restrictions apply to Spartan-6 LX25 and LX25T devices, which is detailed in:

http://www.xilinx.com/support/answers/34885.htm.

New Pin Assignment and Banking Rules

The new pin assignment and banking rules are documented in Appendix B, DRCs, of the PlanAhead User Guide (UG632), and include VCCaux reporting for Virtex-6 and newer devices.

Write I/O STANDARDs to Exported UCF

PlanAhead now has the option to write out all I/O STANDARD constraints to an exported UCF file with the File > Export > Export I/O Ports command.

New and Modified Design Rule Checks

The following is a list of the new and modified Design Rule Check (DRCs) in PlanAhead release 13.

Attribute DRCs

- AVAL—Checks for invalid attribute values on Netlist instances.
- ADEF—Checks for undefined attribute values on Netlist instances.

Bank DCI Cascade DRC

- DCICIOSTD—Checks that the DCI Cascade constraint is legal.

Bank I/O Standard DRC

- VCCAUX2—Warns of any requirements on LVPECL_33 and TMDS_33.

ChipScope DRCs

- CSUC—Checks for unconnected channels on ILA cores.
- CSCL—Checks for non-clock nets that are clocking the capture of probed nets.
- CSBR—Checks if device block RAM resources exceeded.

DSP48 DRCs

- DPCA—Checks the DSP48 cascade to ensure it is feasible based on Netlist connectivity.
- DPREG—Checks for DSP48 asynchronous feedback.

FIFO DRC

- FSYN—Checks for synchronous FIFO.

IOB DRC

- IOPCSLR—Checks for part compatibility between monolithic and SLR/SLL devices.

Placer DRCs

- PLCR—Checks that the number of global clocks in a region is less than the value allowed by the device.
- PLCK—Checks all clock placement rules run during the placer.
- PLDL—Placement constraint for I/Os that checks whether all I/O are locked and whether all members of a bus are locked.
- PLVP—Checks for non-place-able instances due to resource conflicts or limitations.

RAMB DRC

- RAMB—Checks for clock restrictions for READ_FIRST mode.

Required Pin DRC

- REQP—Checks for required pins that are not connected on instances in the netlist.

Implementation Enhancements

PlanAhead 13 contains the following Implementation enhancements:

- Ease of file ordering for Implementation Runs.
- Ability to store Run-specific constraints in a specified UCF file.

Once you implement a design, PlanAhead automatically loads/stores the constraints from that Run in a run-specific UCF.

Reference Documents

The following documents are referenced in this Chapter:

- **Floorplanning Methodology Guide** (UG633):

http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_2/Floorplanning_Methodology_Guide.pdf

- **Hierarchical Design Methodology Guide** (UG748):

http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_2/Hierarchical_Design_Methodology_Guide.pdf

- **ISE Design Suite: Installation and Licensing Guide** (UG798):

http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_2/iil.pdf

- **ISim User Guide** (UG660):

http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_2/plugin_ism.pdf

- **Partial Reconfiguration User Guide** (UG702):

http://www.xilinx.com/tools/partial-reconfiguration.htm

- **PlanAhead Tutorials**:

http://www.xilinx.com/support/documentation/dt_planahead_planahead13_2_tutorials.htm

- **PlanAhead Tcl Command Reference** (UG789):

http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_2/ug793_tcl_commands.pdf

- **PlanAhead User Guide** (UG632):

http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_2/PlanAhead_UserGuide.pdf

- **Power Methodology Guide** (UG786):

http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_2/UG786_PowerMethodolgy.pdf

Known Issues

A list of known issues is compiled in the Answer Record (AR) link at:

http://www.xilinx.com/support/answers/40512.htm

XILINX®

Chapter 3

Architecture Support and Requirements

This chapter describes the operating systems and architectures that the ISE® Design Suite 13 software supports. It also describes system requirements for ISE Design Suite 13. This chapter comprises the following sections:

- Operating Systems
- Architectures
- Compatible Third-Party Tools
- System Requirements

Operating Systems

ISE Design Suite 13 supports three operating systems: Microsoft Windows®, Red Hat® Enterprise Linux, and SUSE Linux Enterprise.

Microsoft Windows

The following table lists Microsoft Windows support.

Table 3-1: **Microsoft Windows Support (English and Japanese)**

Product	XP Professional (32 & 64 bit)	7 Professional (32 & 64 bit)
Design Entry and Implementation Tools (ISE Design Suite Logic Edition 13 software)	Yes	Yes
ISE Simulator (ISim) software	Yes	Yes
ISE WebPACK™ software	Yes	Yes
ChipScope™ Pro software and ChipScope Pro Serial I/O Toolkit	Yes	Yes
Embedded Development Kit (EDK)	Yes	Yes
System Generator for DSP software	Yes	Yes

Linux Support

The following table lists Linux support.

Table 3-2: **Linux Support**

Product	Red Hat Enterprise 4 Workstation (32 & 64 bit)	Red Hat Enterprise 5 Workstation (32 & 64 bit)	SUSE Linux Enterprise (32 & 64 bit)
Design Entry and Implementation Tools (ISE Design Suite 13 software)	Yes	Yes	Yes
ISE Simulator (ISim) software	Yes	Yes	Yes
ISE WebPACK software	Yes	Yes	Yes
ChipScope Pro software and ChipScope Pro Serial I/O Toolkit	Yes	Yes	Yes
Embedded Development Kit (EDK)	Yes	Yes	Yes
System Generator for DSP software	Yes	Yes	Yes

Architectures

ISE Design Suite 13 supports the Virtex® device, Spartan® device, and CPLD device architecture families. The following table lists the architecture support.

Table 3-3: **Architecture Support**

	ISE WebPACK software	ISE Design Suite (Logic Edition, Embedded Edition, DSP Edition, System Edition)
Virtex Series	Virtex-4 devices: LX: XC4VLX15, XC4VLX25 SX: XC4VSX25 FX: XC4VFX12 Virtex-5 devices: LX: XC5VLX30, XC5VLX50 LXT: XC5VLX20T, XC5VLX30T, XC5VLX50T FXT: XC5VFX30T Virtex-6 devices: LXT: XC6VLX75T, XC6VLX75TL Virtex-7 devices: None	Virtex-4 devices: LX: All SX: All FX: All Virtex-5 devices: LX: All LXT: All SXT: All TXT: All FXT: All ***Note:*** Embedded Development Kit (EDK) does not support Virtex-5 TXT devices. Virtex-6 devices: LX/T: All including "L" (lower power) devices CXT: All SXT: All including "L" devices HXT: All ***Note:*** Embedded Development Kit (EDK) does not support Virtex-6 HXT devices. Virtex-7 devices: All
Kintex Series	Kintex-7 devices: XC7K30T XC7K70T XC7K160T	Kintex-7 devices: All

Table 3-3: **Architecture Support**

	ISE WebPACK software	ISE Design Suite (Logic Edition, Embedded Edition, DSP Edition, System Edition)
Spartan Series	Spartan-3 devices: XC3S50 - XC3S1500 Spartan-3A devices: All Spartan-3AN devices: All Spartan-3A DSP devices: XC3SD1800A Spartan-3E devices: All Spartan-3L devices: XC3S1000L, XC3S1500L XA* Spartan-3 devices: All XA* Spartan-3E devices: All XA* Spartan-3A devices: All XA* Spartan-3A DSP devices: XC3SD1800A Spartan-6 devices: LX: XC6SLX4(L)-XC6SLX75(L) LXT: XC6SLX25T, XC6SLX45T, XC6SLX75T XA* Spartan-6 devices: All *Xilinx Automotive	Spartan-3 devices: All Spartan-3A devices: All Spartan-3AN devices: All Spartan-3A DSP devices: All Spartan-3E devices: All Spartan-3L devices: All XA* Spartan-3 devices: All XA* Spartan-3E devices: All XA* Spartan-3A devices: All XA* Spartan-3A DSP devices: All Spartan 6 device: LX/T: All including "L" (lower power) devices XA* Spartan-6 devices: All *Xilinx Automotive
CoolRunner™ XPLA3 devices CoolRunner-II devices XA* CoolRunner-II devices *Xilinx Automotive	All	All ***Note:*** Embedded Development Kit (EDK) does not support CPLDs.
XC9500 Series devices	All (Except 9500XV family)	All (Except 9500XV family) ***Note:*** Embedded Development Kit (EDK) does not support CPLDs.

Compatible Third-Party Tools

Third-Party Tool	Red Hat Linux	Red-Hat Linux-64	SUSE Linux	Windows XP 32-bit	Windows XP-64 bit	Windows-7 32-bit	Windows-7 64-bit
Simulation							
Mentor Graphics ModelSim SE (6.6d)	√	√	√	√	√	√	√
Mentor Graphics ModelSim PE (6.6d)	N/A	N/A	N/A	√	√	√	√
Mentor Graphics ModelSim DE (6.6d)	√	√	√	√	√	√	√

Third-Party Tool	Red Hat Linux	Red-Hat Linux-64	SUSE Linux	Windows XP 32-bit	Windows XP-64 bit	Windows-7 32-bit	Windows-7 64-bit
Mentor Questa (6.6d)	√	√	√	√	√	√	√
Cadence Incisive® Enterprise Simulator (IES) (10.2)	√	√	√	N/A	N/A	N/A	N/A
Synopsys VCS® and VCS MX (2010.06)	√	√	√	N/A	N/A	N/A	N/A
The MathWorks MATLAB® (2009b, 2010a)	√	√	√	√	√	√	√
The MathWorks Simulink® with Fixed-Point Toolbox (2009b, 2010a)	√	√	√	√	√	√	√
Synthesis							
Synopsys Synplify®/Synplify Pro (E-2010.09)	√	√	√	√	√	√	√
Mentor Graphics Precision® RTL/Plus (2010a)	√	√	√	√	√	√	√
Equivalence Checking							
Cadence Encounter® Conformal® (9.1)	√	√	√	N/A	N/A	N/A	N/A

System Requirements

This section provides information on system memory requirements, cable installation, and other requirements and recommendations.

System Memory Recommendations

This section gives the RAM and swap space needed to run ISE Design Suite 13 on your system. The tables below are intended to assist when ordering or building a computer to run FPGA implementation software. These guidelines are based on peak memory requirements for a given device size. For typical memory requirements, please see:

http://www.xilinx.com/ise/products/memory.htm

Memory Requirements Tables

Table 3-4: **Peak Memory Requirements: 32-bit OS**

Memory: 32-bit OS	Family	Device Size
2GB	Spartan-3	3S50 - 3S2000
	Spartan-6	6S4 - 6S45
	Virtex-4	4V12 - 4V25
	Virtex-5	5V20 - 5V50
	Kintex-7	7K30 - 7K70
4GB	Spartan-3	3S3400 - 3S5000
	Spartan-6	6S75 - 6S150
	Virtex-4	4V35 - 4V60
	Virtex-5	5V70 - 5V130
	Virtex-6	6V75
	Kintex-7	7K160

Table 3-5: **Peak Memory Requirements: 64-bit OS**

Memory: 64-bit OS	Family	Device Size
2GB	Spartan-3	3S50 - 3S1400
	Spartan-6	6S4 - 6S16
	Virtex-4	4V12 - 4V25
	Kintex-7	7K30
4GB	Spartan-3	3S1500 - 3S5000
	Spartan-6	6S45
	Virtex-4	4V20 - 4V60
	Virtex-5	5V20 - 5V110
	Virtex-6	6V75
	Kintex-7	7K70 - 7K160
8GB	Virtex-4	4V140 - 4V200
	Virtex-5	5V220 - 5V240
	Virtex-6	6V195 - 6V240
	Kintex-7	7K325

Table 3-5: **Peak Memory Requirements: 64-bit OS**

Memory: 64-bit OS	Family	Device Size
12GB	Virtex-5	5V330
	Virtex-6	6V315 - 6V365
	Kintex-7	7K410
	Virtex-7	7V450 - 7V485
16GB	Virtex-6	6V380 - 6V550
	Virtex-7	7V585 - 7V855
20GB	Virtex-6	6V565 - 6V760
	Virtex-7	7V865 - 7V870
24GB	Virtex-7	7V1500
32GB	Virtex-7	7V2000

Operating Systems and Available Memory

The Microsoft Windows and Linux® operating system (OS) architectures have limitations on the maximum memory available to a Xilinx program. Users targeting the largest devices and most complex designs may encounter this limitation. ISE Design Suite 13 has optimized memory and enabled software support for applications to increase RAM memory available to Xilinx software.

Windows XP Professional 32-bit

Xilinx applications are enabled to take advantage of the memory increase feature on Windows 32-bit. You must then modify Windows setting to get access to this larger memory.

The standard Windows OS architecture limits the maximum memory available to a Xilinx process to 2 Gigabyte (GB). In Windows XP Professional, Microsoft created an option to support the ability of an application to address 3 GB of RAM. Xilinx ISE applications have built-in support for this option. To take advantage of this capability, you must also modify your Windows XP OS to enable this feature, which requires that you modify your `boot.ini` file by adding a "/3GB" entry to the end of the "startup" line.

Before enabling 3 GB support for Xilinx applications, please read the Microsoft Knowledge Base Article #328269 at http://support.microsoft.com/?kbid=328269. If you upgrade your computer to Windows XP Service Pack 1 (SP1) and you are using the /3GB switch, Windows may not restart without a patch from Microsoft. Please see (Xilinx Answer 17905) for more information.

Additionally, before making this change, please read:

- Microsoft Bulletin Q17193 http://support.microsoft.com/default.aspx?scid=kb;en-us;Q171793, which contains information on "Application Use of 4GT RAM Tuning".
- Microsoft Bulletin Q289022 http://support.microsoft.com/default.aspx?scid=kb;en-us;q289022, contains instructions for editing your `boot.ini` file.

Linux

ISE Design Suite 13 supports both Linux 32-bit and Linux 64-bit. The latter allows greater memory allocation. Xilinx has documented Linux kernel modifications that allow a Xilinx application to address over 3 GB of memory.

For 32-bit Red Hat Enterprise Linux systems, the operating system can use the hugemem kernel to allocate 4 GB to each process. More information can be found on the Red Hat support site: http://www.redhat.com/docs/manuals/enterprise/

ISE supports the 64-bit version of Red Hat Enterprise Linux, which allows greater memory allocation out of the box.

Cable Installation Requirements

Platform Cable USB II and Parallel Cable IV are high-performance cables that enable Xilinx® design tools to program and configure target hardware.

To install Platform Cable USB II, a system must have at least a USB 1.1 port. For maximum performance, Xilinx recommends using Platform Cable USB II with a USB 2.0 port.

To install Parallel Cable IV, a system must have a parallel port connector and support parallel port communication.

Cables are officially supported on the 32-bit and 64-bit versions of the following operating systems: Windows XP Professional, Windows-7, Red Hat Linux Enterprise, and SUSE Linux Enterprise 11. Additional platform specific notes are as follows:

- All Linux: Root privileges are required to install cable drivers on Linux.
- SUSE Linux Enterprise 11: The fxload software package is required to ensure correct Platform Cable USB II operation. The fxload package is not automatically installed on SUSE Linux Enterprise 11 distributions, and must be installed by the user or System Administrator.
- Linux LibUSB support: Support for Platform Cable USB II based upon the LibUSB package is now available from the Xilinx website. See Answer Record #29310 for details.

For additional information regarding Xilinx cables, refer to the following documents:

- USB Cable Installation Guide (UG344)
- Platform Cable USB II Data Sheet (DS593)
- Parallel Cable IV Data Sheet (DS097)

Equipment and Permissions

The following table lists related equipment, permissions, and network connections.

Table 3-6: **Equipment and Permissions Requirements**

Item	Requirement
Directory permissions	Write permissions must exist for all directories containing design files to be edited.
Monitor	16-bit color VGA with a minimum recommended resolution of 1024 by 768 pixels.
Drive	You must have a DVD-ROM for ISE Design Suite (if you have received a DVD, rather than downloading from the web), and CD-ROM for MXE on your system. ***Note:*** ModelSim Xilinx Edition and ModelSim Xilinx Edition Starter will no longer be available on CDs or for download beginning December 10th, 2010. Xilinx will also stop generating licenses and providing updated libraries for both products on December 10th, 2010. This means that ISE® Design Suite 12.3 was the last version of Xilinx ISE software to support ModelSim Xilinx Edition-III. Please see Product Discontinuance Notice XCN10028 for more details.
Ports	To program devices, you must have an available parallel, or USB port appropriate for your Xilinx programming cable. Specifications for ports are listed in the documentation for your cable. ***Note:*** Installation of the cable driver software requires Windows XP Pro SP1 (or later), or Windows-7. If you are not using one of these operating systems, the cables may not work properly.

Note: X Servers/ Remote Desktop Servers, such as Exceed, ReflectionX, and XWin32, are not supported.

Network Time Synchronization

When design files are located on a network machine, other than the machine with the installed software, the clock settings of both machines must be set the same. These times must be synchronized on a regular basis for continued proper functioning of the software.

ChipScope Pro Analyzer

Cable Installation Requirements

For Linux, cable drivers require root privileges to install. To install Platform Cable USB II for USB 2.0 port, you must have Windows XP SP2. The Platform Cable USB II is a high-performance download cable that attaches to user hardware for use with the ChipScope Pro Analyzer tool for device programming, configuring, and debugging.

System Memory Recommendations

The ChipScope Pro Analyzer software requires 1024 megabytes (MB) of system memory. The ChipScope Pro Core Inserter tool has the same requirements as ISE. For more

information on ISE memory recommendations, see:
http://www.xilinx.com/ise/products/memory.htm.

System Generator for DSP System Requirements and Recommendations

Hardware Recommendations

Table 3-7: **System Generator for DSP Hardware Recommendations**

Recommendation	Notes
4.00 GB of RAM	N/A
600 MB of hard disk space	Minimum Requirement
Xilinx Hardware Co-Simulation Platform	Required for the Hardware Co-Simulation Flow

OS and Software Requirements

Table 3-8: **System Generator for DSP OS and Software Requirements**

Requirement	Notes
Windows XP Professional SP2, 32-bit/64-bit or Windows-7, 32-bit/64-bit or Red Hat Linux 5.2, 32-bit & 64-bit	N/A
Xilinx ISE Design Suite 13.2	N/A
MathWorks MATLAB Version 2010a or 2010b. Beta support for MATLAB Version 2011a.	N/A
MathWorks Simulink with Fixed-Point Toolbox Version 2010a or 2010b. Beta support for MathWorks Simulink with Fixed-Point Toolbox Version 2011a.	MATLAB must be installed in a directory with no spaces (e.g., C:\MATLAB\R2010a) The Fixed-Point Toolbox is required if a Gateway Out block has an output greater than 53 bits. Signals internal to the Xilinx Gateway In and Gateway Out blocks can be larger than 53 bits without needing the Fixed-Point Toolbox.

XILINX®

Chapter 4

Technical Support, Services, and Documentation

This chapter describes how to access technical support, services, and documentation that are available. This chapter contains the following sections:

Technical Support

For technical questions, visit the Xilinx® support site,

www.xilinx.com/support/

where you can search the Answers Database or utilize the following self support features:

- Download Center, www.xilinx.com/support/download/index.htm
- Answer Browser, www.xilinx.com/support/answers/index.htm
- Xilinx User Community Forums, http://forums.xilinx.com
- Design Resources - Video Demonstrations, www.xilinx.com/design

If you cannot resolve your issue using our online resources, you can contact Xilinx Technical Support directly at:

www.xilinx.com/support/techsup/tappinfo.htm

Education Services

Xilinx provides targeted, high-quality education services designed by experts in programmable logic design, and delivered by Xilinx qualified trainers. Available are onsite and online instructor led courses, and recorded e-learning for self paced learning.

For more information on training courses, free on-demand training, live online training, and upcoming events, visit the Xilinx Training website,

www.xilinx.com/support/education-home.htm

Documentation

Xilinx offers technical documentation to assistant users with using the ISE® Design Suite tools.

Context-Sensitive Help

Context-sensitive online Help is available for most ISE Design Suite tools that are available with a graphical user interface (GUI). From Project Navigator, select **Help > Help Topics** to access the online Help.

Software Manuals

Detailed software manuals about the ISE Design Suite applications and command-line functions are included as part of the software installation. After you install the software, you can select the **Help > Software Manuals** command in Project Navigator to access the software manuals collection.

Note: If you do not already have Adobe Acrobat Reader installed, you must do so to view the software manuals.

A new documentation navigation page is now the default startup page in Xilinx Platform Studio (XPS). From the documentation tab you can browse to all Embedded Development Kit (EDK) documentation. From outside XPS, open the file `edk_documentation_locator.htm`, which is found at `$XILINX_EDK/doc`.

To locate the Software Manuals on the website:

1. Go to the Documentation Center, http://www.xilinx.com/support/
2. Click the **Design Tools** tab.
3. Click the Design Tool category, such as ISE, or click the **See All Design Tools Documentation** link.

User Tutorials

Tutorials can be found online at:

http://www.xilinx.com/support/techsup/tutorials/index.htm

Third-Party Licenses

The Third-Party Licenses govern the use of certain third-party technology included in and/or distributed in connection with the Xilinx ISE® Design Suite software tools. Each license applies only to the applicable technology expressly governed by such license and not to any other technology.

To view the Third-Party Licenses details, see the Xilinx Third-Party Licenses Guide.