ACPL-K453
High Speed Optocoupler

AVAGO TECHNOLOGIES

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

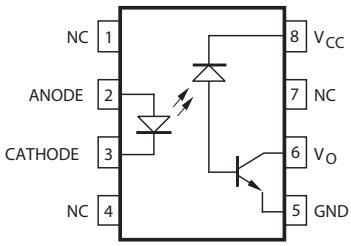
Description

The ACPL-K453 is a single channel devices in an eight lead miniature footprint.

This diode-transistor optocoupler uses an insulating layer between the light emitting diode and an integrated photo detector to provide electrical insulation between input and output. Separate connections for the photodiode bias and output transistor collector increase the speed up to a hundred times over that of a conventional photo-transistor coupler by reducing the base-collector capacitance.

The ACPL-K453 has a common mode transient immunity of 15,000 V/µs minimum at V_{CM} = 1500 V guaranteed.

Functional Diagram

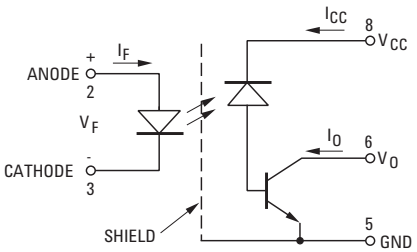


TRUTH TABLE

LED	V_O
ON	LOW
OFF	HIGH

A 0.1 µF bypass capacitor between pins 5 and 8 is recommended.

Schematic



Features

- Package Clearance/Creepage at 8mm
- Function Compatible with HCPL-4503
- Surface Mountable in 8-pin stretched SO8
- Very High Common Mode Transient Immunity: 15000 V/µs at V_{CM} = 1500 V Guaranteed
- High Speed: 1 Mb/s
- TTL Compatible
- Guaranteed AC and DC Performance over Temperature: 0°C to 70°C
- Open Collector Output
- Safety approval
  UL Recognized 5000 Vrms for 1 minute per UL1577
  CSA Approved
  IEC/EN/DIN EN 60747-5-2 Approved V_{IORM} = 1140 V peak

Applications

- Line Receivers - High common mode transient immunity (>15000 V/µs) and low input-output capacitance (0.6 pF).
- High Speed Logic Ground Isolation - TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL.
- Replace Slow Phototransistor Optocouplers
- Replace Pulse Transformers - Save board space and weight
- Analog Signal Ground Isolation - Integrated photo detector provides improved linearity over phototransistor type.

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Ordering Information

ACPL-K453 is UL Recognized with 5000 Vrms for 1 minute per UL1577 and is approved under CSA Component Acceptance Notice #5, File CA 88324.

Part number	Option RoHS Compliant	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-2	Quantity
ACPL-K453	-000E	Stretched SO-8	X			80 per tube
	-500E		X	X		1000 per reel
	-060E		X		X	80 per tube
	-560E		X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

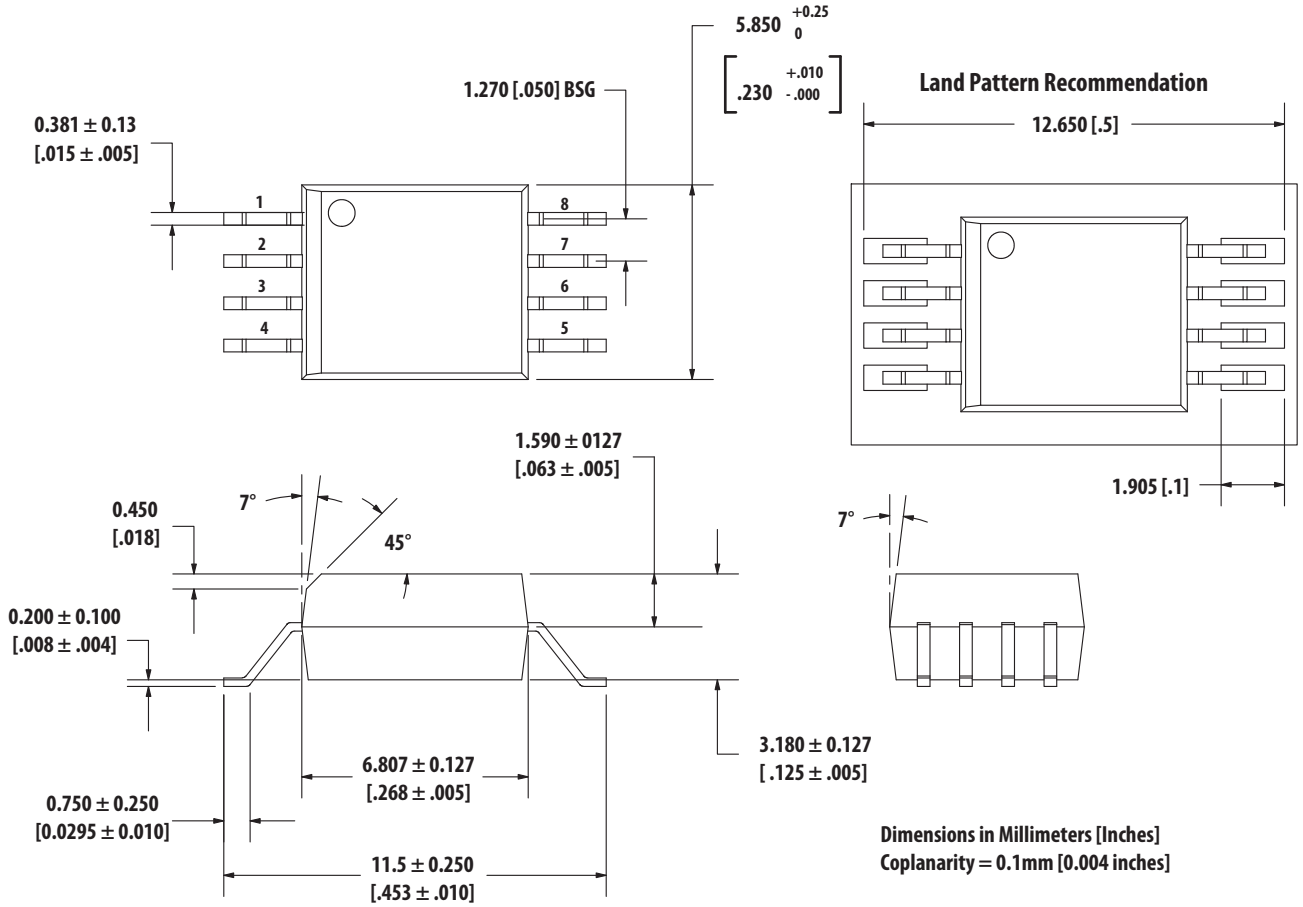
ACPL-K453-560E to order product of Stretched SO-8 package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-2 Safety Approval in RoHS compliant.

Example 2:

ACPL-K453to order product of Stretched SO-8 package in tube packaging and RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Outline Drawing (Stretched SO8)



Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

The ACPL-W453 are pending approval by the following organizations:

IEC/EN/DIN EN 60747-5-2 (Option 060 only)

Approval under:
IEC 60747-5-2 :1997 + A1:2002
EN 60747-5-2:2001 + A1:2002
DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01

UL - Approval under UL 1577, component recognition program up to V_{ISO} = 5000 V_{RMS}. File E55361.

CSA - Approval under CSA Component Acceptance Notice #5, File CA 88324.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min External Air Gap (Clearance)	L(IO1)	8	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L(IO2)	8	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

IEC/EN/DIN EN 60747-5-2 Insulation Related Characteristics (Option 060 only)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 300 V rms		I-IV	
for rated mains voltage ≤ 450 V rms		I-III	
for rated mains voltage ≤ 600 Vrms		I-III	
for rated mains voltage ≤ 1000 Vrms		I-II	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1140	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec Partial Discharge < 5 pC,	V_{PR}	2137	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	1710	V_{peak}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	8000	V_{peak}
Safety Limiting Values (Maximum values allowed in the event of a failure)			
Case Temperature	T_S	175	°C
Input Current	$I_{S,INPUT}$	230	mA
Output Power	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	10^9	Ω

* Refer to the optocoupler section of the Designer's Catalog, under regulatory information (IEC/EN/DIN EN 60747-5-2) for a detailed description of Method a and Method b partial discharge test profiles.

Absolute Maximum Ratings

Parameter	Abs. Max.
Storage Temperature	-55°C to +125°C
Operating Temperature	-55°C to +100°C
Average Input Current - I_F	25 mA[1]
Peak Input Current - I_F	50 mA[2] (50% duty cycle, 1 ms pulse width)
Peak Transient Input Current - I_F	1.0 A (≤1 ms pulse width, 300 pps)
Reverse Input Voltage - V_R (Pin 3-2)	5 V
Input Power Dissipation	45 mW[3]
Average Output Current - I_O (Pin 6)	8 mA
Peak Output Current	16 mA
Output Voltage - V_O (Pin 6-5)	-0.5 V to 20 V
Supply Voltage - V_{CC} (Pin 8-5)	-0.5 V to 30 V
Output Power Dissipation	100 mW[4]
Solder Reflow Temperature Profile	see Package Outline Drawings section

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions			Fig.	Note
Current Transfer Ratio	CTR	19	24	50	%	T_A = 25°C	V_O = 0.4 V	V_{CC} = 4.5 V, VI_F = 16 mA	1, 2, 4	5
		15	25				V_O = 0.5 V			
Logic Low Output Voltage	V_{OL}		0.1	0.4	V	T_A = 25°C	I_O = 3.0 mA			
				0.5			I_O = 2.4 mA			
Logic High Output Current	I_{OH}		0.003	0.5	µA	T_A = 25°C	V_O = V_{CC} = 5.5 V	I_F = 0 mA	7	
			0.01	1		T_A = 25°C	V_O = V_{CC} = 15.0 V			
				50						
Logic Low Supply Current	I_{CCL}		50	200		I_F = 16 mA, V_O = Open, V_{CC} = 15 V				10
Logic High Supply Current	I_{CCH}		0.02	1		T_A = 25°C	I_F = 16 mA, V_O = Open, V_{CC} = 15 V			10
				2						
Input Forward Voltage	V_F		1.5	1.7	V	T_A = 25°C	I_F = 16 mA		3	
Input Reverse Breakdown Voltage	BV_R	5				I_R = 10 µA				
Temperature Coefficient of Forward Voltage	$\Delta V_F / \Delta T_A$		-1.6		mV/°C	I_F = 16 mA				
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0				

*All typicals at T_A = 25°C.

Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C) V_{CC} = 5 V, I_F = 16 mA unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}		0.2	0.8	µs	T_A = 25°C	R_L = 1.9 kΩ, C_L = 15 pF	5,6,9	9
				1.0					
Propagation Delay Time to Logic High at Output	t_{PLH}		0.6	0.8		T_A = 25°C	R_L = 1.9 kΩ, C_L = 15 pF	5,6,9	9
				1.0					
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	15	30		kV/µs	V_{CM} =1500 V_{p-p}	I_F = 0 mA, T_A = 25°C R_L = 1.9 kΩ, C_L = 15 pF	10	8,9
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	15	30			V_{CM} =1500 V_{p-p}	I_F = 16 mA, T_A = 25°C R_L = 1.9 kΩ, C_L = 15 pF	10	8,9

* All typicals at T_A = 25°C.

Package Characteristics

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified. All typicals at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	5000			Vrms	RH ≤ 50%, t = 1 min; T_A = 25°C		6,7
Input-Output Resistance	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 Vdc		6
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz; V_{I-O} = 0 Vdc		6

* The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table (if applicable).

Notes:

1. Derate linearly above 85°C free-air temperature at a rate of 0.5 mA/°C.
2. Derate linearly above 85°C free-air temperature at a rate of 1.0 mA/°C.
3. Derate linearly above 85°C free-air temperature at a rate of 1.1 mW/°C.
4. Derate linearly above 85°C free-air temperature at a rate of 2.3 mW/°C.
5. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100.
6. Device considered a two terminal device: pins 2 and 3 shorted together, and pins 5, 6, 7 and 8 shorted together.
7. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{RMS} for 1 second (leakage detection current limit, I_{I-O} ≤ 5 µA).
8. Common transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the rising edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the falling edge of the common mode pulse signal, V_{CM} to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
9. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
10. Use of a 0.1 mF bypass capacitor connected between pins 4 and 6 is recommended.

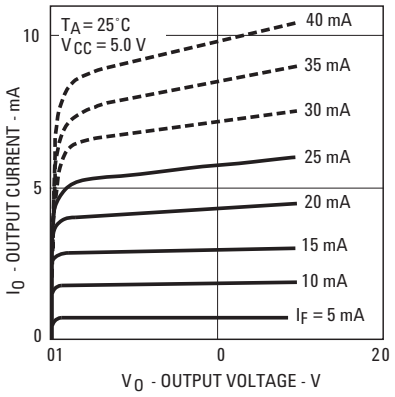


Figure 1. dc and Pulsed Transfer Characteristics.

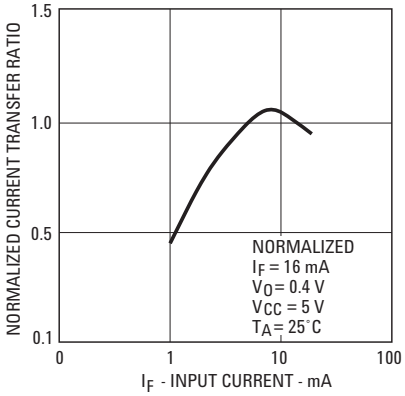


Figure 2. Current Transfer Ratio vs. Input Current.

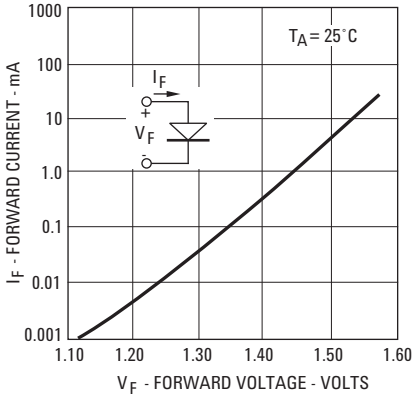


Figure 3. Input Current vs. Forward Voltage.

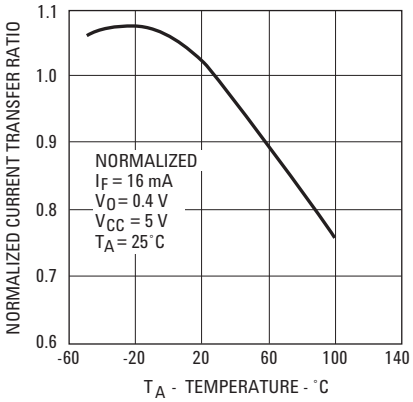


Figure 4. Current Transfer Ratio vs. Temperature.

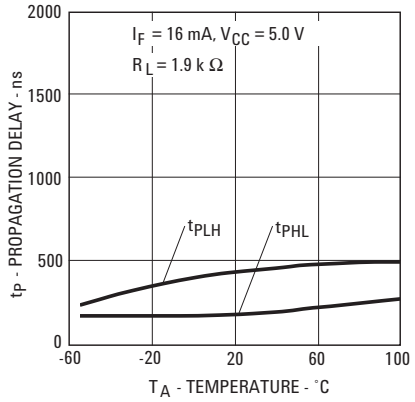


Figure 5. Propagation Delay vs. Temperature.

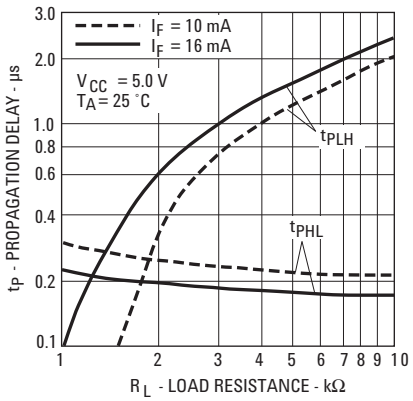


Figure 6. Propagation Delay Time vs. Load Resistance.

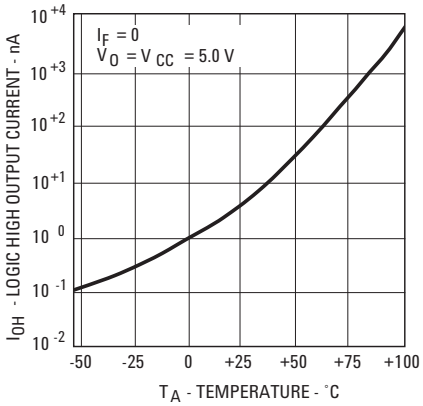


Figure 7. Logic High Output Current vs. Temperature.

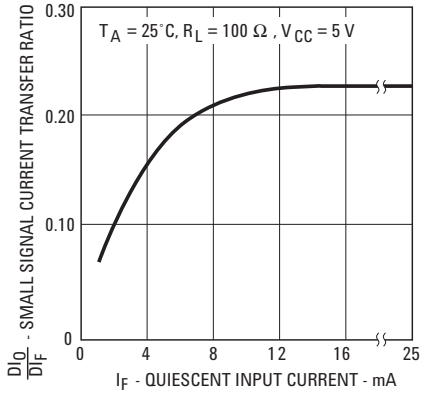


Figure 8. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.

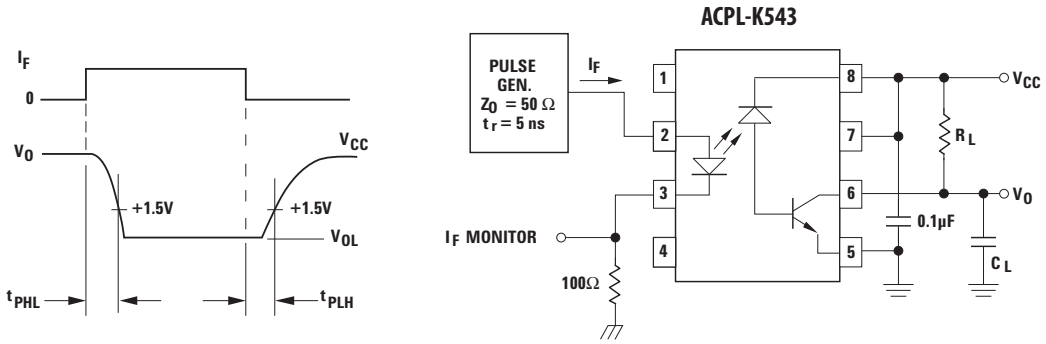


Figure 9. Switching Test Circuit.

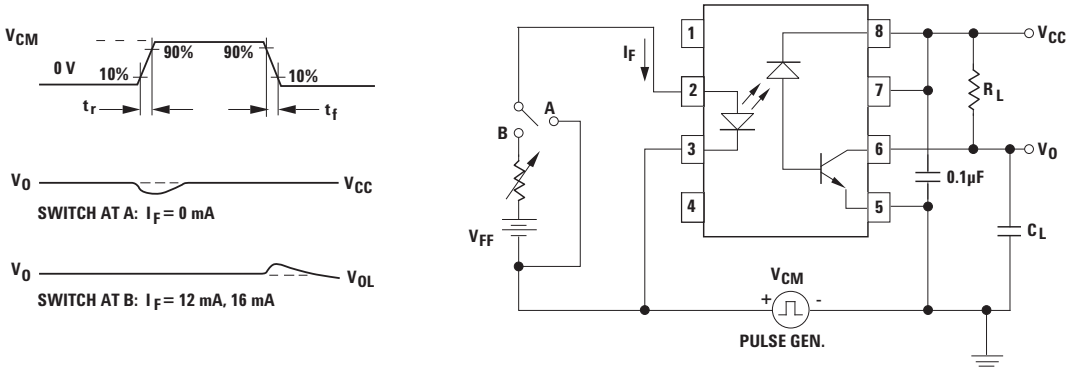


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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