

FDMJ1032C

Dual N & P-Channel PowerTrench® MOSFET N-Channel: 20V, 3.2A, 90mΩ P-Channel: -20V, -2.5A, 160mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 90mΩ at $V_{GS} = 4.5V$, $I_D = 3.2A$
- Max $r_{DS(on)}$ = 130mΩ at $V_{GS} = 2.5V$, $I_D = 2.5A$

Q2: P-Channel

- Max $r_{DS(on)}$ = 160mΩ at $V_{GS} = -4.5V$, $I_D = -2.5A$
- Max $r_{DS(on)}$ = 230mΩ at $V_{GS} = -2.5V$, $I_D = -2.0A$
- Max $r_{DS(on)}$ = 390mΩ at $V_{GS} = -1.8V$, $I_D = -1.0A$
- Low gate charge, high power and current handling capability
- RoHS Compliant



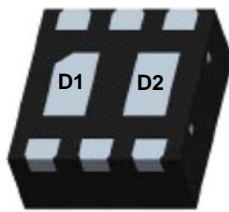
General Description

This dual N and P-Channel enhancement mode Power MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

Application

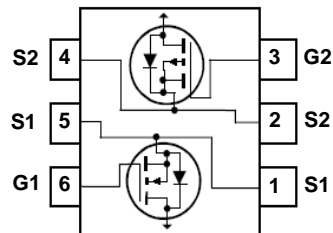
- Battery management

Pin 1 → S1 S2 G2



G1 S1 S2
SC-75 MicroFET

Bottom Drain Contact



Bottom Drain Contact

MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V_{DS}	Drain to Source Voltage	20	-20	V
V_{GS}	Gate to Source Voltage	± 12	± 8	V
I_D	Drain Current - Continuous $T_A = 25^\circ\text{C}$	3.2	-2.5	A
	- Pulsed	12	-12	
P_D	Power Dissipation for Single Operation $T_A = 25^\circ\text{C}$	(Note 1a)	1.4	W
		(Note 1b)	0.8	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Single Operation (Note 1a)	89	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Single Operation (Note 1b)	182	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
032	FDMJ1032C	SC-75 MicroFET	7"	8mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$ $I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	Q1 Q2	20 -20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C $I_D = -250\mu\text{A}$, referenced to 25°C	Q1 Q2		13 -13		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{V}, V_{GS} = 0\text{V}$ $V_{DS} = -16\text{V}, V_{GS} = 0\text{V}$	Q1 Q2			1 -1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{V}, V_{DS} = 0\text{V}$ $V_{GS} = \pm 8\text{V}, V_{DS} = 0\text{V}$	Q1 Q2			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$ $V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	Q1 Q2	0.6 -0.4	1.1 -0.8	1.5 -1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C $I_D = -250\mu\text{A}$, referenced to 25°C	Q1 Q2		-3 3		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 4.5\text{V}, I_D = 3.2\text{A}$ $V_{GS} = 2.5\text{V}, I_D = 2.5\text{A}$ $V_{GS} = 4.5\text{V}, I_D = 3.2\text{A}, T_J = 125^\circ\text{C}$	Q1		70 100 83	90 130 132	m Ω
		$V_{GS} = -4.5\text{V}, I_D = -2.5\text{A}$ $V_{GS} = -2.5\text{V}, I_D = -2.0\text{A}$ $V_{GS} = -1.8\text{V}, I_D = -1.0\text{A}$ $V_{GS} = -4.5\text{V}, I_D = -2.5\text{A}, T_J = 125^\circ\text{C}$	Q2		114 169 289 156	160 230 390 238	m Ω
g_{FS}	Forward Transconductance	$V_{DD} = 5\text{V}, I_D = 3.2\text{A}$	Q1		7.5		S
		$V_{DD} = -5\text{V}, I_D = -2.5\text{A}$	Q2		5		

Dynamic Characteristics

C_{iss}	Input Capacitance	Q1 $V_{DS} = 10\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	Q1 Q2		200 290	270 390	pF
C_{oss}	Output Capacitance	Q2	Q1 Q2		50 55	70 75	pF
C_{riss}	Reverse Transfer Capacitance	$V_{DS} = -10\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	Q1 Q2		30 29	45 45	pF
R_g	Gate Resistance	$f = 1\text{MHz}$	Q1		1		Ω
			Q2		5		

Switching Characteristics

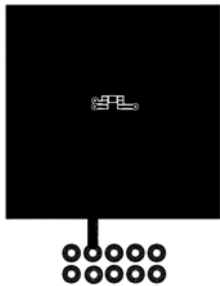
$t_{d(on)}$	Turn-On Delay Time	Q1 $V_{DD} = 10\text{V}, I_D = 1\text{A},$ $V_{GS} = 4.5\text{V}, R_{GEN} = 6\Omega$	Q1 Q2		7 8	14 16	ns
t_r	Rise Time		Q1 Q2		8 13	16 23	ns
$t_{d(off)}$	Turn-Off Delay Time	Q2 $V_{DD} = -10\text{V}, I_D = -1\text{A},$ $V_{GS} = -4.5\text{V}, R_{GEN} = 6\Omega$	Q1 Q2		11 13	20 23	ns
t_f	Fall Time		Q1 Q2		2 18	4 32	ns
$Q_{g(TOT)}$	Total Gate Charge	Q1 $V_{GS} = 4.5\text{V}, V_{DD} = 10\text{V}, I_D = 3.2\text{A}$	Q1 Q2		2 3	3 4	nC
Q_{gs}	Gate to Source Charge		Q1 Q2		0.4 0.6		nC
Q_{gd}	Gate to Drain "Miller" Charge	Q2 $V_{GS} = -4.5\text{V}, V_{DD} = -10\text{V}, I_D = -2.5\text{A}$	Q1 Q2		1.0 0.8		nC

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

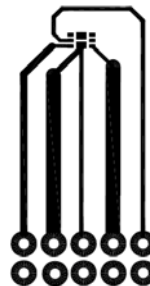
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics							
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0V, I_S = 1.16A$ (Note 2)	Q1		0.8	1.2	V
		$V_{GS} = 0V, I_S = -1.2A$ (Note 2)	Q2		-0.8	-1.2	
t_{rr}	Reverse Recovery Time	Q1 $I_F = 3.2A, di/dt = 100A/s$	Q1		12		ns
			Q2		14		
Q_{rr}	Reverse Recovery Charge	Q2 $I_F = -2.5A, di/dt = 100A/s$	Q1		2.5		nC
			Q2		4		

Notes:

- $R_{\theta JA}$ is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 89°C/W when mounted on a 1 in² pad of 2 oz copper



b. 182°C/W when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

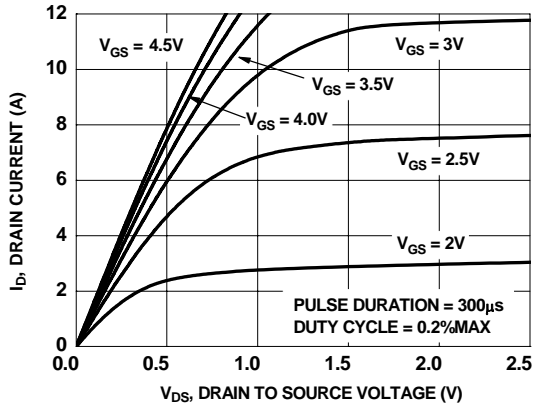


Figure 1. On-Region Characteristics

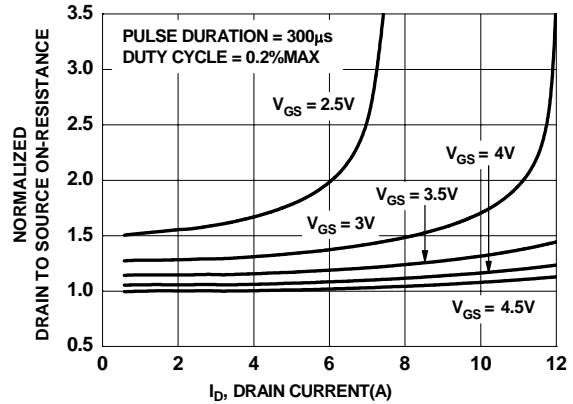


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

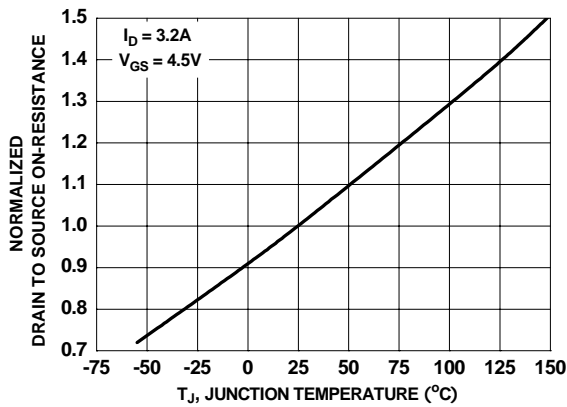


Figure 3. Normalized On-Resistance vs Junction Temperature

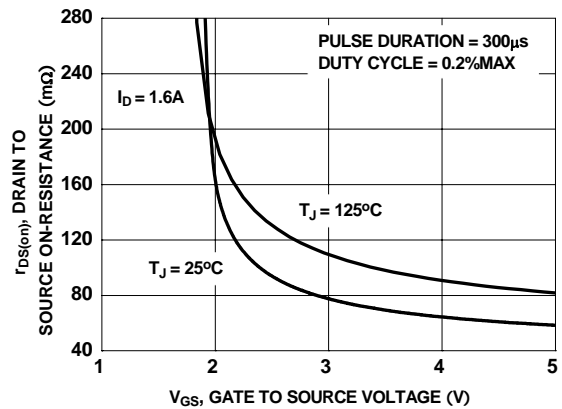


Figure 4. On-Resistance vs Gate to Source Voltage

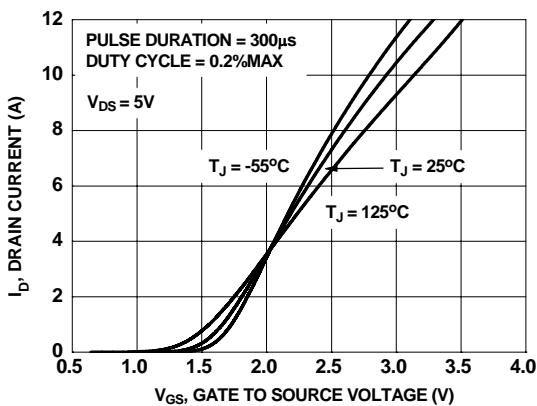


Figure 5. Transfer Characteristics

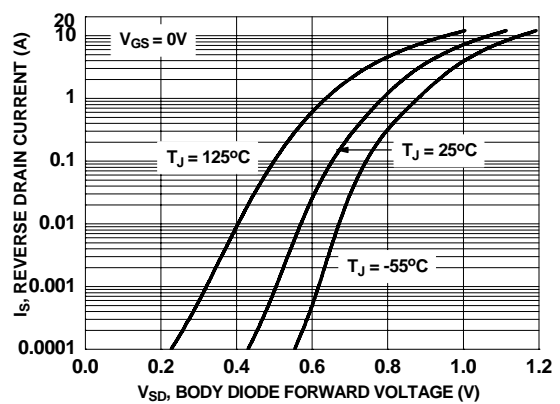


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

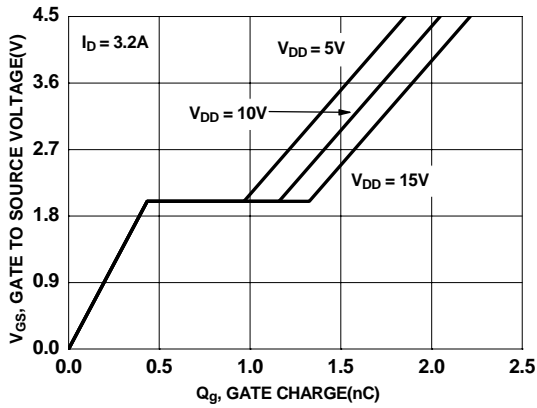


Figure 7. Gate Charge Characteristics

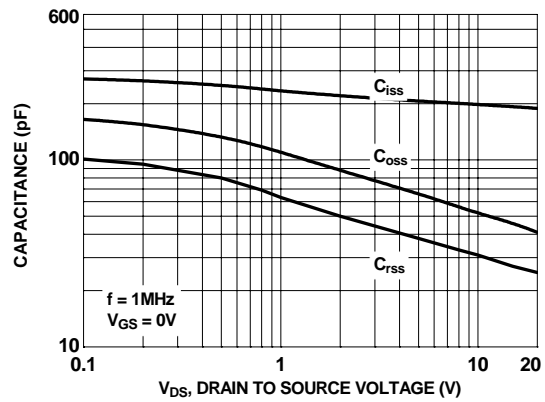


Figure 8. Capacitance vs Drain to Source Voltage

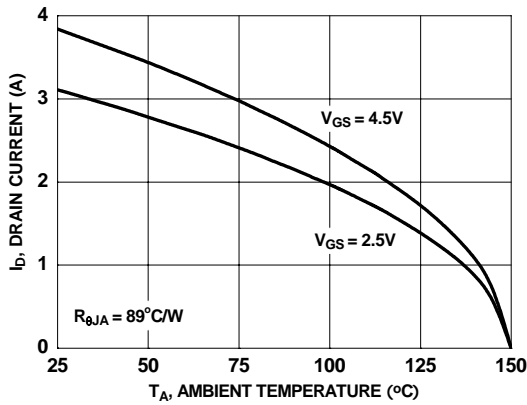


Figure 9. Maximum Continuous Drain Current vs Ambient Temperature

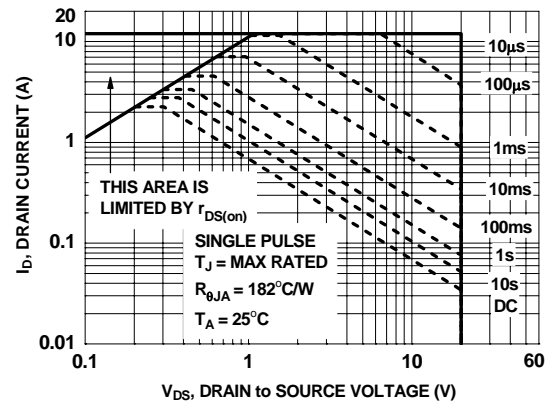


Figure 10. Forward Bias Safe Operating Area

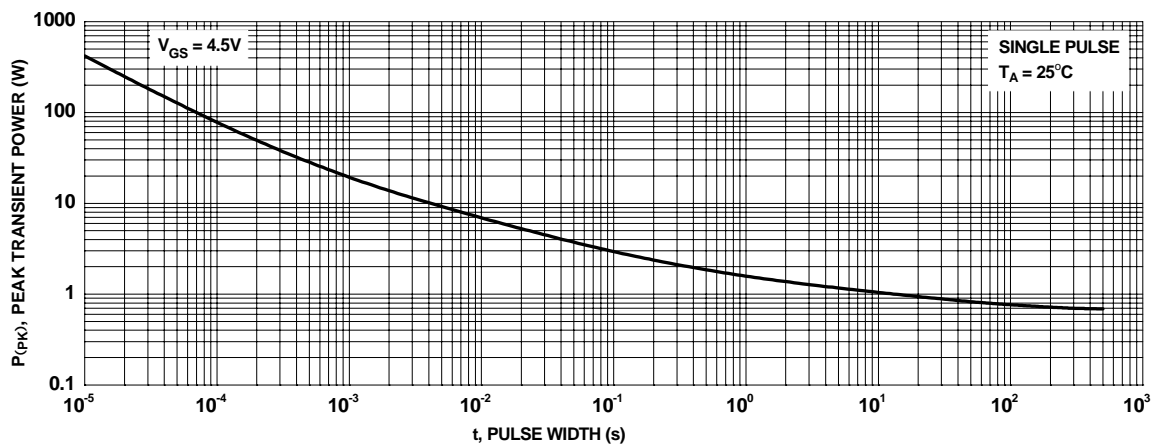


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

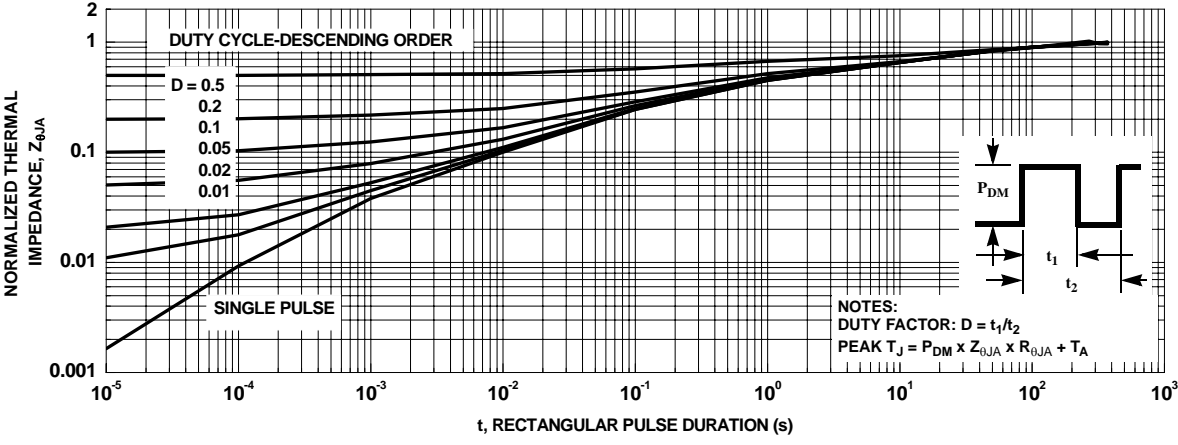


Figure 12. Transient Thermal Response Curve

Typical Characteristics (Q2 P-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

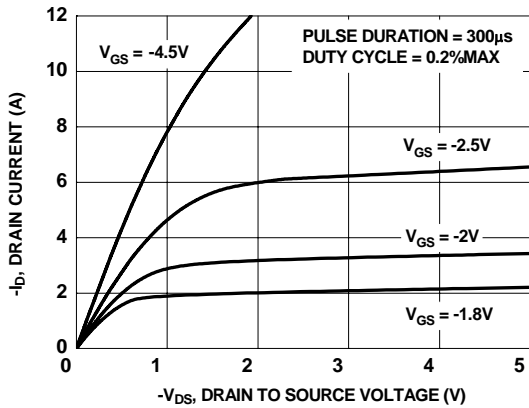


Figure 13. On- Region Characteristics

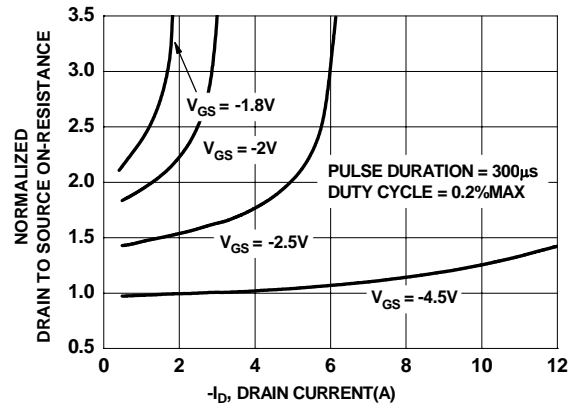


Figure 14. Normalized on-Resistance vs Drain Current and Gate Voltage

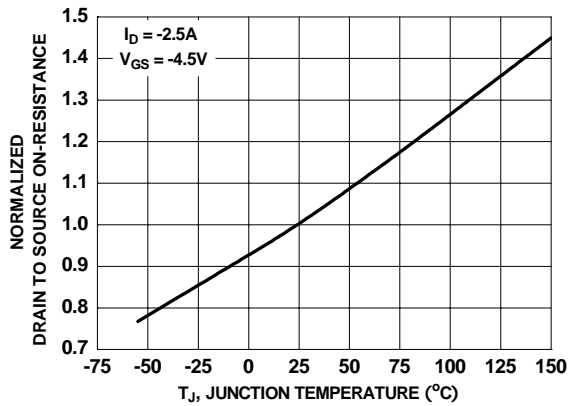


Figure 15. Normalized On-Resistance vs Junction Temperature

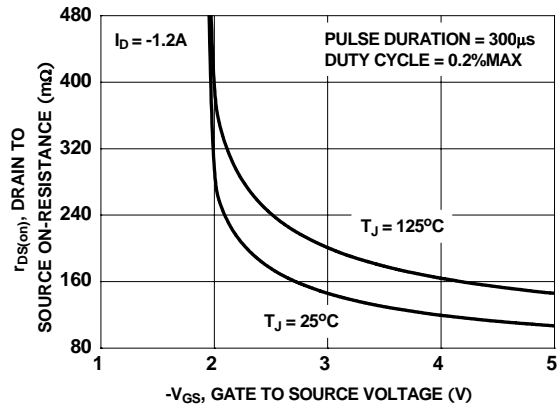


Figure 16. On-Resistance vs Gate to Source Voltage

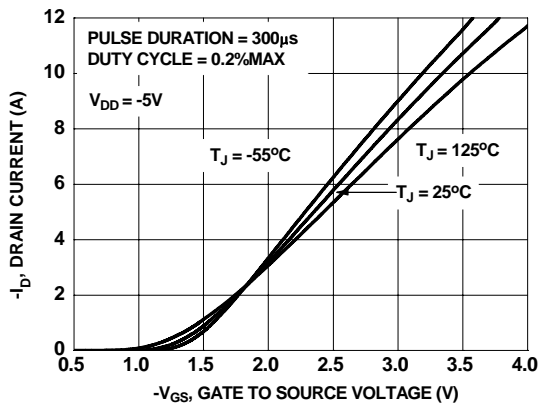


Figure 17. Transfer Characteristics

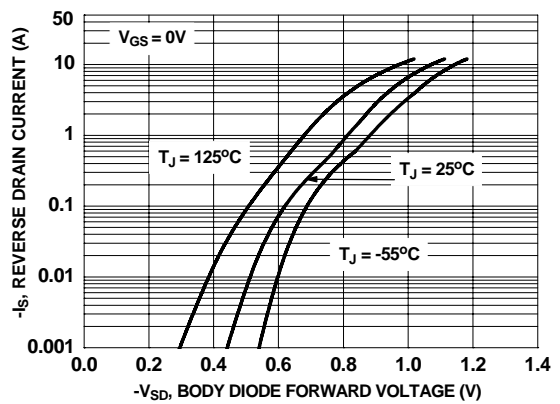


Figure 18. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 P-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

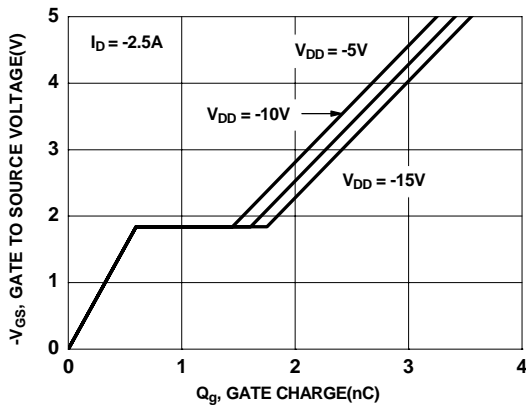


Figure 19. Gate Charge Characteristics

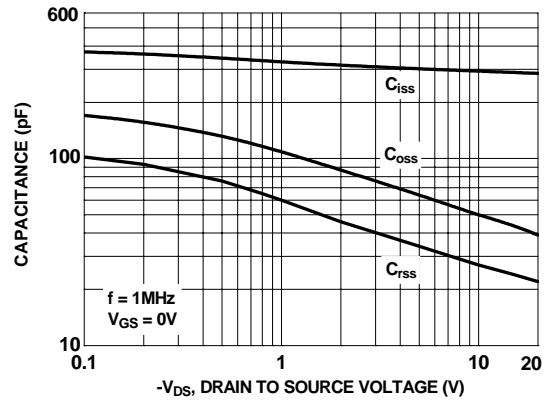


Figure 20. Capacitance vs Drain to Source Voltage

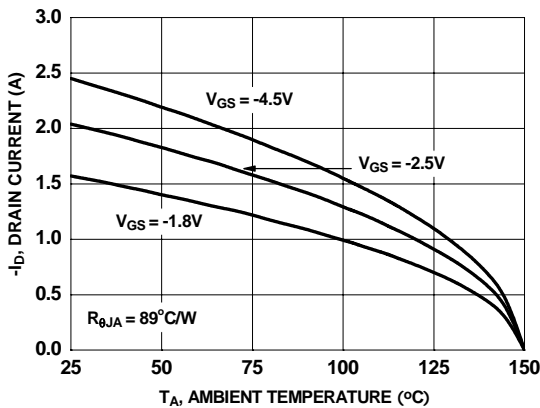


Figure 21. Maximum Continuous Drain Current vs Ambient Temperature

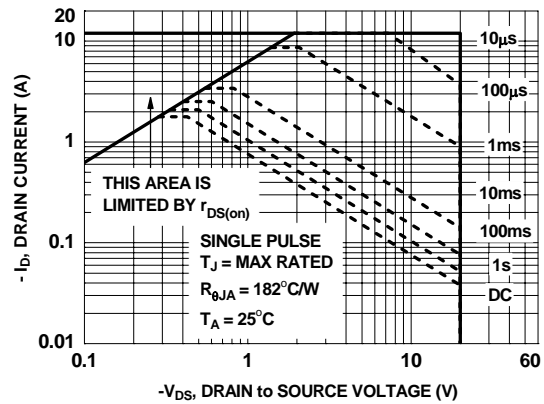


Figure 22. Forward Bias Safe Operating Area

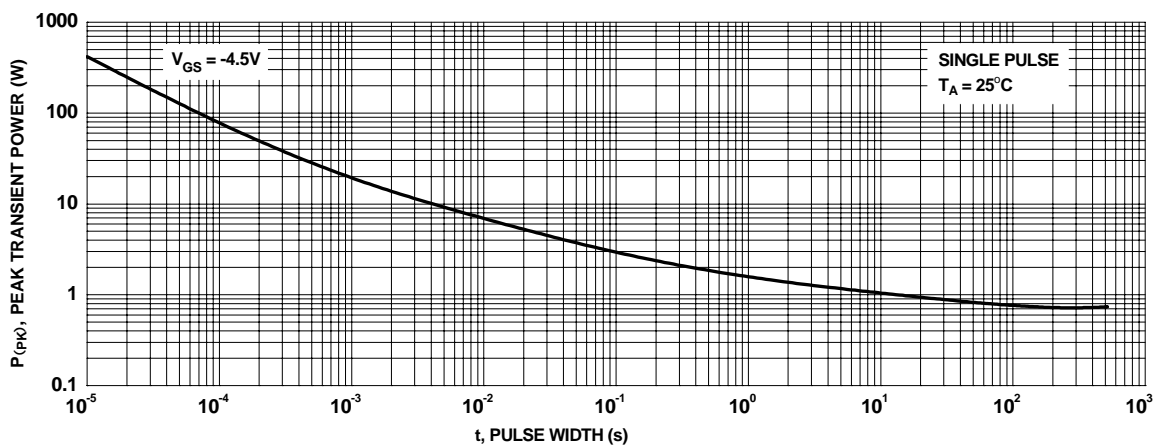


Figure 23. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 P-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

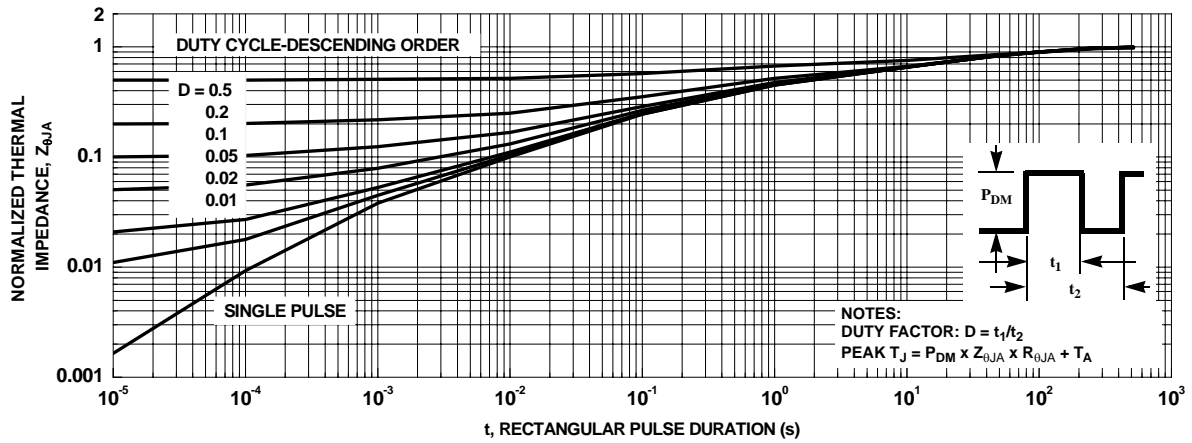



Figure 24. Transient Thermal Response Curve



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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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