AN994
Application note

L638xE application guide

Introduction

STMicroelectronics' L638xE is a versatile, high-voltage gate driver family of devices.

Developed using BCD offline technology, the L6384E, L6385E, L6386E, L6387E and L6388E devices can operate with high voltage rails up to 600 V. The gate drivers provide all the functions and current capability necessary for high- and low-side power MOSFETs and IGBTs.

The devices can be used in all types of applications where high-voltage shifted control is necessary; they have a relatively high driver current capability and are provided with an internal patented circuitry that replaces the external bootstrap diode. This feature is achieved by means of a high voltage DMOS, synchronously driven with the low-side gate driver.

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1 L6384E

The L6384E (depicted in *Figure 1*) is a half-bridge driver with an externally-adjustable dead time and shut-down function. To disable the driver, the control pin (DT/SD at pin 3) must be pulled down to below 0.5 V. The dead time can be set from 0.5 µs to 2.7 µs by placing a resistor between pin 3 and ground. Available in both Minidip and SO-8 packages, this driver can be used in motor controls, resonant converters and lighting applications. *Figure 2* and *Figure 3* show the schematic diagram of the evaluation circuit and the layout of the test PCB.

Table 1. L6384E pin description

N.	Name	Typ.	Function
1	IN(1)	I	Logic input. In phase with HVG and in opposition to LVG. Compatible with the V_{CC} voltage.
2	V_{cc}		Supply input voltage. Includes an internal clamp (typically 15.6 V). Also has a UVLO feature (typical threshold value V_{ccth1} = 12 V, V_{ccth2} = 10 V).
3	DT/SD	I	High impedance pin with double function. When pulled to a voltage lower than V_{dt} (typically 0.5 V) the device is shut down. A voltage higher than V_{dt} sets the dead time between the high side and low side gate driver. The dead time value can be set by forcing a certain voltage level on the pin or by connecting a resistor between pin 3 and ground. Care must be taken to avoid spikes on pin 3 that could cause an undesired shut down of the IC. For this reason, the connection of the components between pin 3 and ground must be as short as possible. This pin cannot be left floating for the same reason. The pin must not be pulled through a low impedance to V_{CC} because of the drop on the current source that feeds R_{dt}.
4	GND		Ground.
5	LVG	O	Low-side driver output. The output stage can deliver a 400 mA source and a 650 mA sink (typical values). The circuit guarantees 0.3 V maximum on the pin (at I_{sink}= 10 mA) with V_{CC} > 3 V and lower than the turn-on threshold. This removes the need for the bleeder resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low. The gate driver ensures low impedance in SD conditions as well.
6	OUT	O	Upper driver floating reference. Attention should be paid to the layout design of the power stage so as to limit below-ground spikes on this pin.
7	HVG	O	High-side driver output. The output stage can deliver a 400 mA source and a 650 mA sink (typical values). The circuit guarantees 0.3 V maximum between this pin and Vout (at I_{sink} = 10 mA) with V_{CC} > 3 V and lower than the turn-on threshold. This removes the need for the bleeder resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low. The gate driver ensures low impedance in SD conditions as well.
8	V_{BOOT}		Bootstrap supply voltage. This is the upper driver floating supply. The bootstrap capacitor connected between this pin and pin 6 can be fed by an internal structure named "bootstrap driver" (a patented structure). This structure can replace the external bootstrap diode.

1. The pull-down internal resistor is typically some hundred kΩs.

Figure 1. L6384E internal block diagram

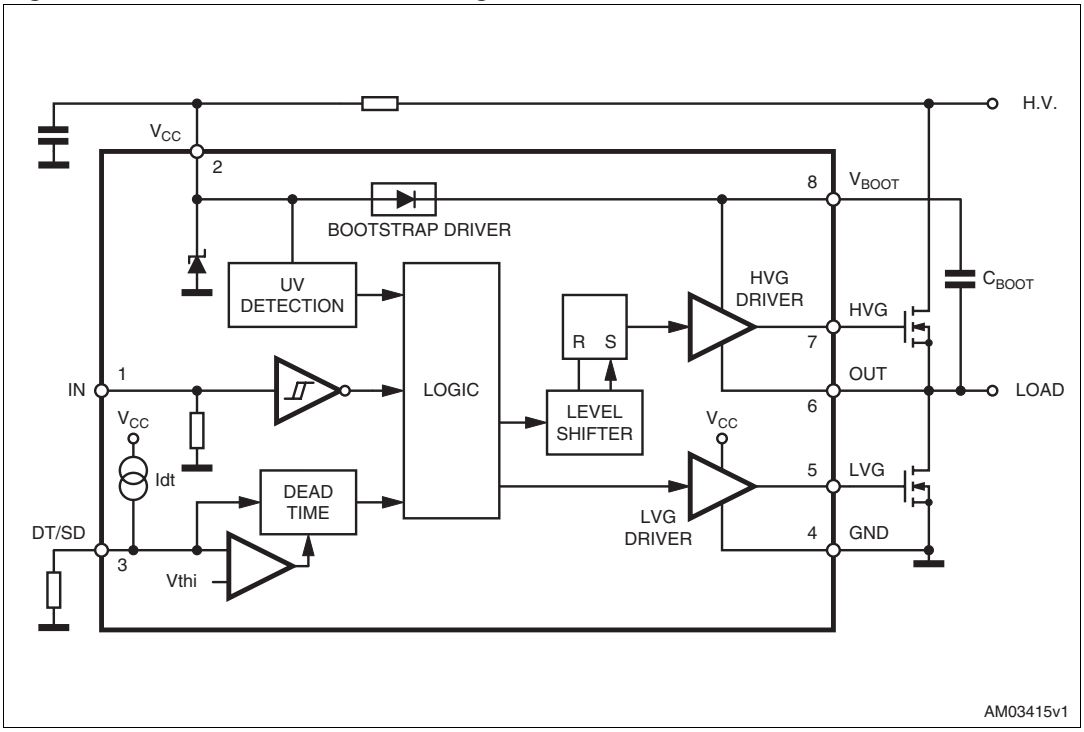


Figure 2. L6384E - schematic diagram of the evaluation circuit

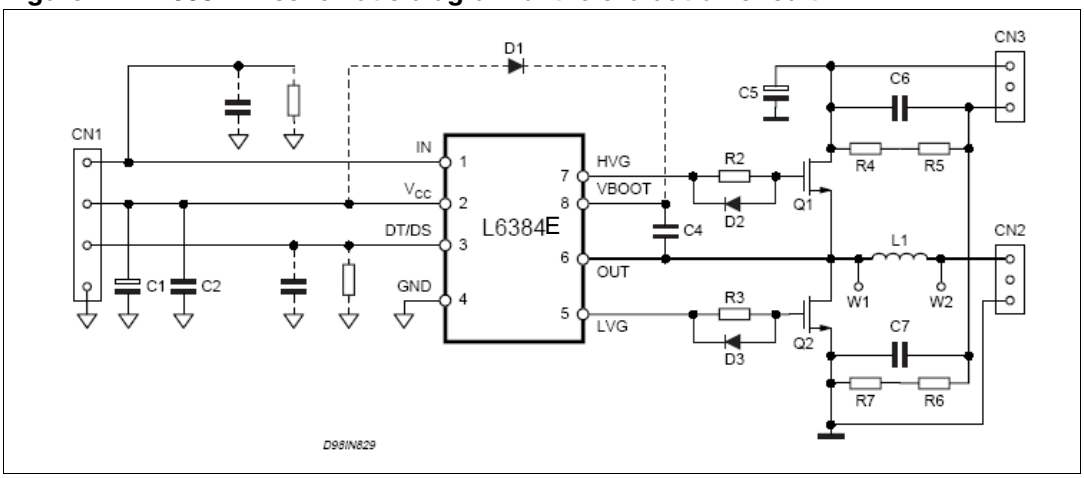
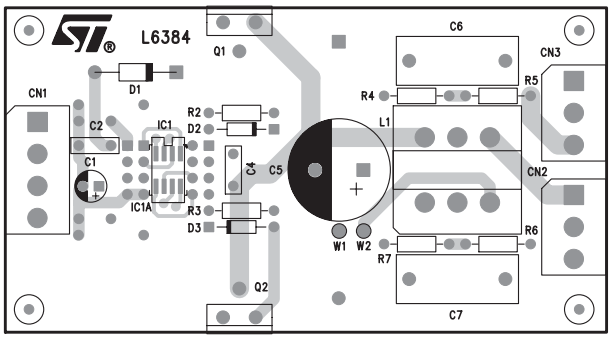
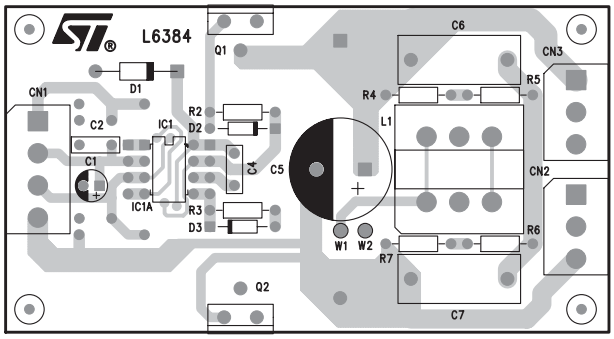


Figure 3. L6384E - PCB and component layout of the evaluation circuit



Top view



Bottom view

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2 L6385E

The L6385E (shown in *Figure 4*) is a high- and low-side configurable driver. It can control the high- and low-side outputs (HVG and LVG) seperately, through the two related logic inputs HIN and LIN. This device is provided with an undervoltage detection function in both the low voltage V_{CC} supply and high-voltage bootstrapped supply. Delivered in 8-pin packages, this driver has been specifically designed for power supplies and motion control applications.

Figure 5 and *Figure 6* show the schematic diagram of the evaluation circuit and the layout of the relevant PCB.

Table 2. L6385E pin description

N.	Name	Type	Function
1	LIN (1)	I	Low-side driver logic input. Compatible with the V_{CC} voltage ($V_{il\ Max}$ = 1.5 V, $V_{ih\ Min}$ = 3.6 V)
2	HIN (1)	I	High-side driver logic input. Compatible with the V_{CC} voltage ($V_{il\ Max}$ = 1.5 V, $V_{ih\ Min}$ = 3.6 V)
3	Vcc		Supply input voltage with UVLO (typically V_{ccth1} = 9.6 V, V_{ccth2} = 8.3 V).
4	GND		Ground.
5	LVG	O	Low-side driver output. The output stage can deliver a 400 mA source and a 650 mA sink (typical values). The circuit guarantees 0.3 V maximum on the pin (at Isink = 10 mA) with V_{CC} > 3 V and lower than the turn-on threshold. This removes the need for the bleeder resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low. The gate driver ensures low impedance in SD conditions as well.
6	OUT	O	High-side driver floating reference. Attention should be paid to the layout design of the power stage so as to limit below-ground spikes on this pin.
7	HVG	O	High-side driver output. The output stage can deliver a 400 mA source and a 650 mA sink (typical values). The circuit guarantees 0.3 V maximum between this pin and Vout (at Isink = 10 mA) with V_{CC} > 3 V and lower than the turn-on threshold. This removes the need for the bleeder resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low.
8	V_{BOOT}		Bootstrap supply voltage. This is the floating supply of the high-side driver. Includes a UVLO function (typically, V_{BSth1} = 9.5 V, V_{BSth2}= 8.2 V). The bootstrap capacitor connected between this pin and pin 6 can be fed by an internal structure named "bootstrap driver" (a patented structure). This structure can replace the external bootstrap diode.

1. The pull-down internal resistor is typically some hundred kΩs.

Figure 4. L6385E - internal block diagram

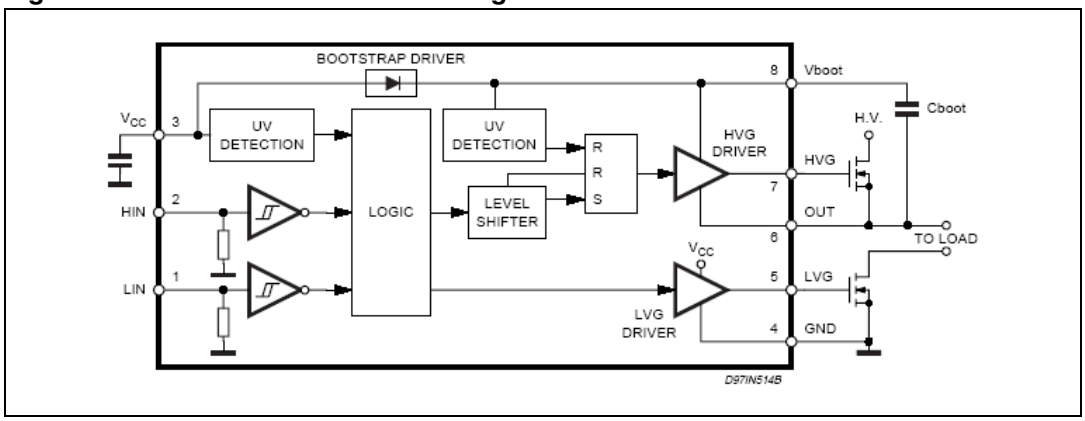


Figure 5. L6385E - schematic diagram of the evaluation circuit

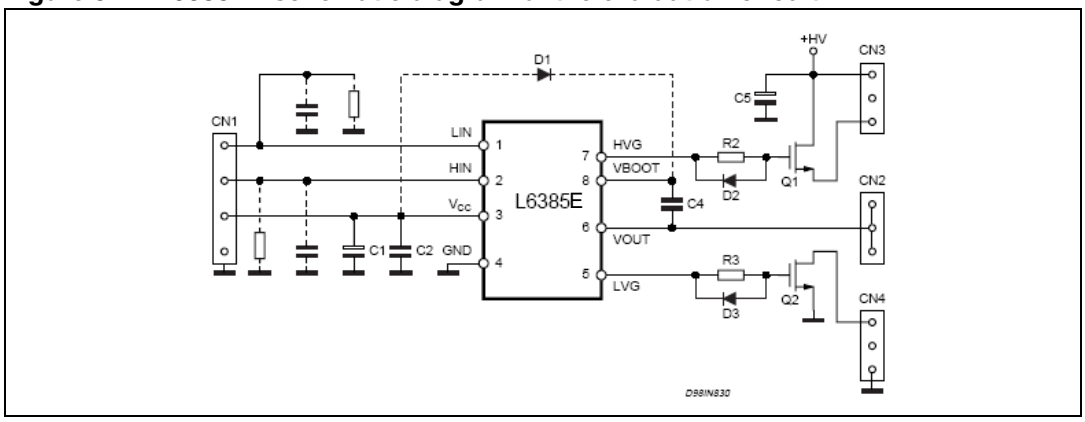
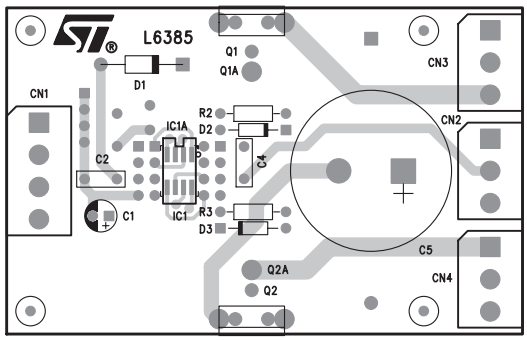


Figure 6. L6385E - PCB and component layout of the evaluation circuit



3 L6386E

The L6386E (shown in *Figure 7*) is a configurable driver based on the structure of the L6385E, with added functions. This device is available in DIP14 or SO-14 packages.

The added shutdown function (active low) and the current sense comparator (0.5-V threshold) with diagnostic output, make this device particularly suitable for motion control applications with cycle-by-cycle current feedback. The DIAG and CIN pins can be used to stop the device (by acting on the SD pin). *Figure 8* and *Figure 9* show the schematic diagram of the evaluation circuit and the layout of the relevant PCB.

Table 3. L6386E pin description

N.	Name	Type	Function
1	LIN (1)	I	Lower driver logic input. Compatible with the V_{CC} voltage ($V_{il\ Max}$ = 1.5 V, $V_{ih\ Min}$ = 3.6 V).
2	SD (1)	I	Shut-down logic input. Compatible with the V_{CC} voltage. If it needs to be pulled up, the suggested resistor value is 5 to 10 kΩ. ($V_{il\ Max}$ = 1.5 V, $V_{ih\ Min}$ = 3.6 V).
3	HIN (1)	I	Low-side driver logic input. Compatible with the V_{CC} voltage.
4	Vcc		Supply input voltage with UVLO (typically V_{ccth1} = 12 V, V_{ccth2} = 10 V).
5	DIAG	O	Diagnostic output: open drain.
6	CIN	I	Comparator input.
7	SGND		Ground reference for logic signals.
8	PGND		Power ground reference for the low voltage gate driver.
9	LVG	O	Low-side driver output. The output stage can deliver a 400 mA source and a 650 mA sink (typical values). The circuit guarantees 0.3 V maximum on the pin (at I_{sink} = 10 mA) with V_{CC} > 3 V and lower than the turn-on threshold. This removes the need for the bleeder resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low. The gate driver ensures low impedance in SD conditions as well.
10, 11	N.C.		Not connected.
12	OUT	O	High-side floating driver. Attention should be paid to the layout design of the power stage so as to limit below-ground spikes on this pin.
13	HVG	O	High-side driver output. The output stage can deliver a 400 mA source and a 650 mA sink (typical values). The circuit guarantees 0.3 V maximum between this pin and Vout (at I_{sink} = 10 mA) with V_{CC} > 3 V and lower than the turn-on threshold. This removes the need for the bleeder resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low. The gate driver ensures low impedance in SD conditions as well.
14	V_{BOOT}		Bootstrapped supply voltage. This is the floating supply of the high-side driver. Includes a UVLO function (typically, V_{Bth1} = 11.9V, V_{Bth2} = 9.9 V). The bootstrap capacitor connected between this pin and pin 12 can be fed by an internal structure named "bootstrap driver" (a patented structure). This structure can replace the external bootstrap diode.

1. The pull-down internal resistor is typically some hundred kΩs.

Figure 7. L6386E - internal block diagram

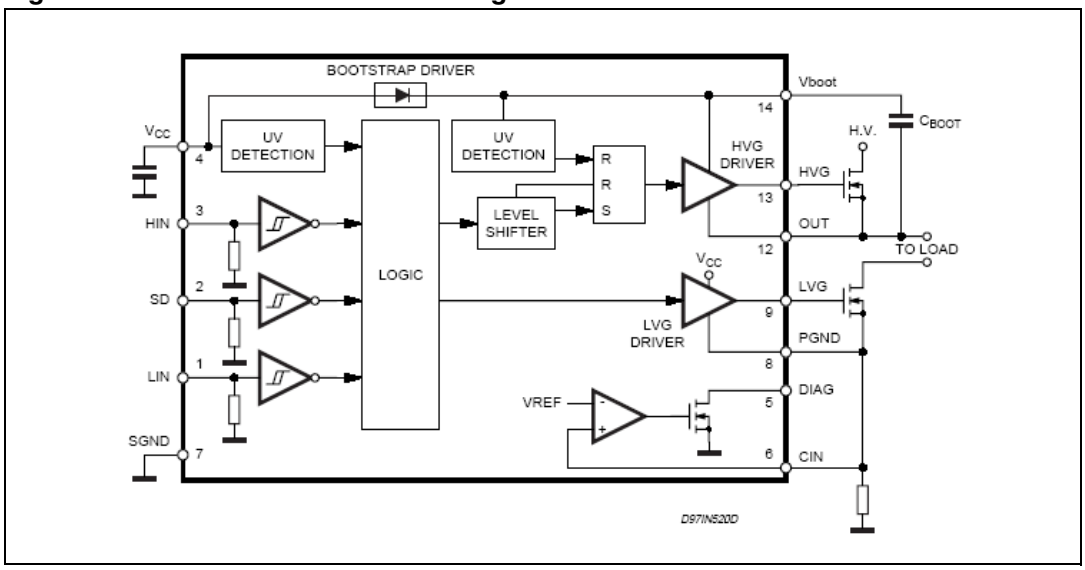


Figure 8. L6386E - schematic diagram of the evaluation circuit

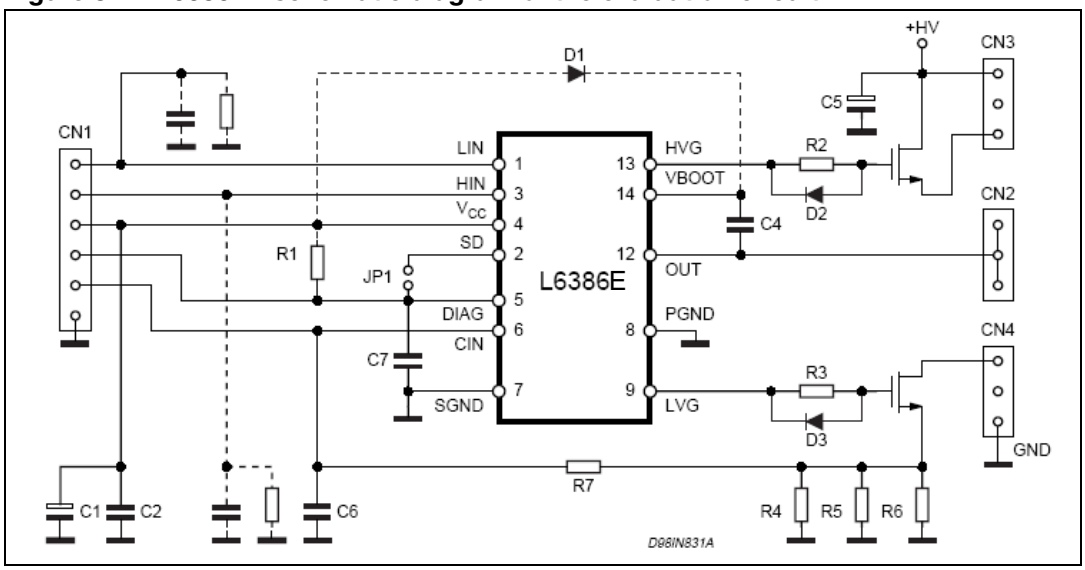
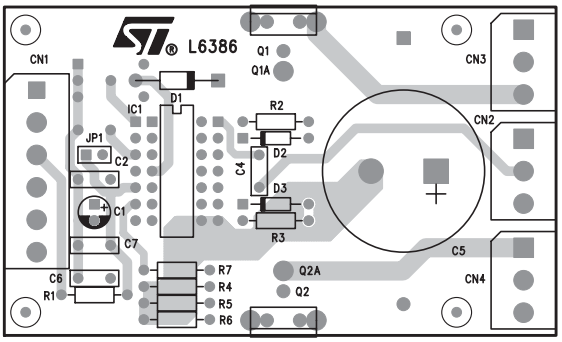
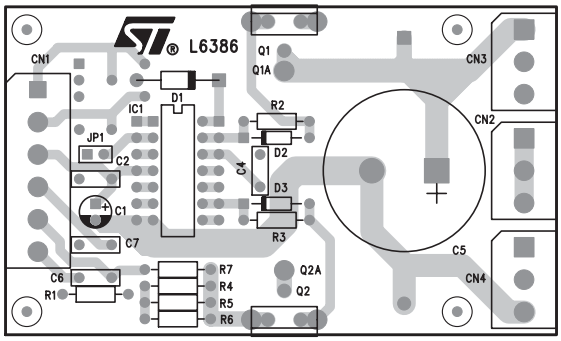


Figure 9. L6386E - PCB and component layout of the evaluation circuit



Top view



Bottom view

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4 L6387E

The L6387E (shown in *Figure 10*) is based on the structure of the L6385E. It has two separate inputs and also includes an interlocking function to avoid both power switches from being unintentionally switched on at the same time (see *Table 5*).

The V_{CC} turn-on and turn-off thresholds have been lowered to 6 and 5.5 V respectively (typical). There is no UVLO on the upper driving section.

The L6387E can be evaluated using the L6385E board.

Table 4. L6387E pin description

N.	Name	Type	Function
1	LIN(1)	I	Low-side driver logic input. Compatible with V_{CC} voltage ($V_{il\ Max}$ = 1.5 V, $V_{ih\ Min}$ = 3.6 V).
2	HIN (1)	I	High-side driver logic input. Compatible with V_{CC} voltage ($V_{il\ Max}$ = 1.5 V, $V_{ih\ Min}$ = 3.6 V).
3	V_{cc}		Supply input voltage (with very low UVLO: V_{ccth1} = 6 V and V_{ccth2} = 5.5 V)
4	GND		Ground.
5	LVG	O	Low-side driver output. The output stage can deliver a 400 mA source and a 650 mA sink (typical values). The circuit guarantees 0.3 V maximum on the pin (at I_{sink} = 10 mA) with V_{CC} > 3 V and lower than the turn-on threshold. This removes the need for the bleeder resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low.
6	OUT	O	High-side driver floating reference. Attention should be paid to the layout design of the power stage so as to limit below-ground spikes on this pin.
7	HVG	O	High-side driver output. The output stage can deliver a 400 mA source and a 650 mA sink (typical values). The circuit guarantees 0.3 V maximum between this pin and Vout (at I_{sink} = 10 mA) with V_{CC} > 3 V and lower than the turn-on threshold. This removes the need for the bleeder resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low.
8	V_{BOOT}		Bootstrap supply voltage. This is the floating supply of the high-side driver. The bootstrap capacitor connected between this pin and pin 6 can be fed by an internal structure named "bootstrap driver" (a patented structure). This structure can replace the external bootstrap diode.

1. The pull-down internal resistor is typically some hundred kΩs.

Figure 10. L6387E - internal block diagram

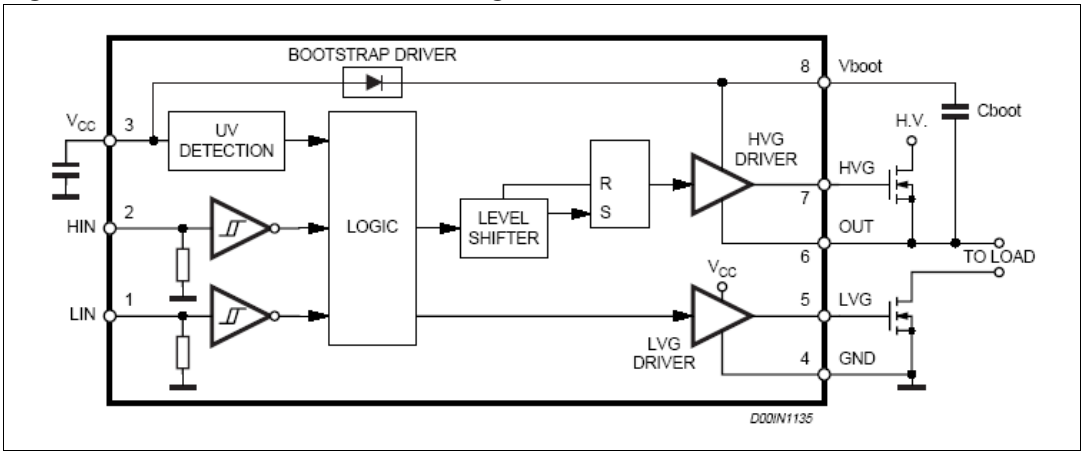


Table 5. Truth table

INPUT	HIN	0	0	1	1
	LIN	0	1	0	1
OUTPUT	HVG	0	0	1	0
	LVG	0	1	0	0

5 L6388E

The L6388E (see *Figure 11*) is based on the structure of the L6385E. It has two separate inputs that are 3.3-V compatible, a fixed dead time of approximately 320 ns and an interlocking function to avoid both power switches from being unintentionally switched on at the same time (see *Table 5*).

The UVLO thresholds of V_{CC} and V_{BOOT} are the same as for the L6385E.

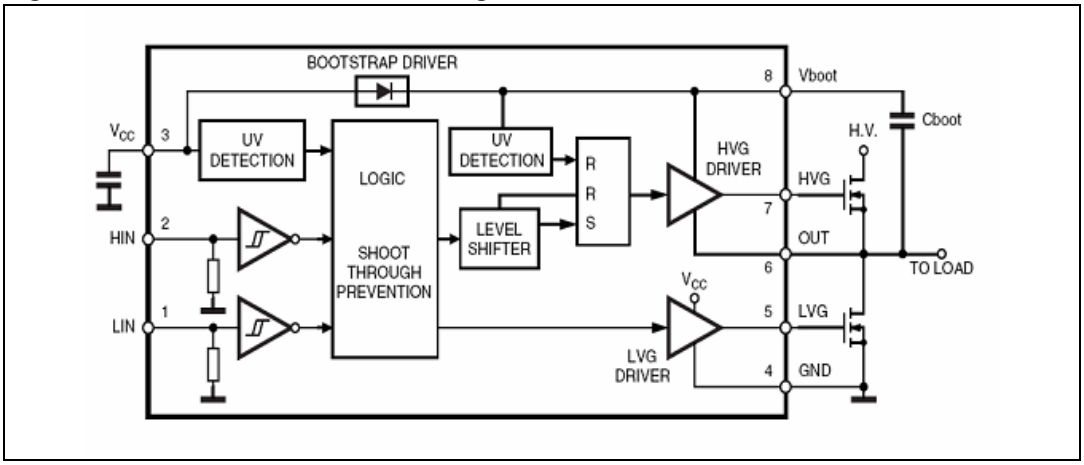
The L6388E can be evaluated using the L6385E board.

Table 6. L6388E pin description

N.	Name	Type	Function
1	LIN (1)	I	Low-side driver logic input. Compatible with the V_{CC} voltage ($V_{il\ Max}$ = 1.1 V, $V_{ih\ Min}$ = 1.8 V).
2	HIN (1)	I	High-side driver logic input. Compatible with the V_{CC} voltage ($V_{il\ Max}$ = 1.1 V, $V_{ih\ Min}$ = 1.8 V).
3	V_{CC}		Supply input voltage with UVLO (typical V_{ccth1} = 9.6 V and typical V_{ccth2} = 8.3 V).
4	GND		Ground
5	LVG	O	Low-side driver output. The output stage can deliver a 400 mA source and a 650 mA sink (typical values). The circuit guarantees 0.3 V maximum on the pin (at I_{sink} = 10 mA) with V_{CC} > 3 V and lower than the turn-on threshold. This removes the need for the bleeder resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low.
6	VOUT	O	High-side driver floating reference. Attention should be paid to the layout design of the power stage so as to limit below-ground spikes on this pin.
7	HVG	O	High-side driver output. The output stage can deliver a 400 mA source and a 650 mA sink (typical values). The circuit guarantees 0.3 V maximum between this pin and V_{out} (at I_{sink} = 10 mA) with V_{CC} >3 V and lower than the turn-on threshold. This removes the need for the bleeder resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low.
8	V_{BOOT}		Bootstrap supply voltage. This is the high-side driver floating supply (with UVLO: typical V_{BSth1} = 9.5 V, V_{BSth2} = 8.2 V). The bootstrap capacitor connected between this pin and pin 6 can be fed by an internal structure named "bootstrap driver" (a patented structure). This structure can replace the external bootstrap diode.

1. The pull-down internal resistor is typically some hundred kΩs.

Figure 11. L6388E internal block diagram



6 Bootstrap driver

A bootstrap circuitry is required to supply the high voltage section. This function is normally accomplished by a high-voltage fast recovery diode (see *Figure 12*). In the L638xE, a patented integrated structure replaces the external diode. This structure is comprised of a high-voltage DMOS—driven synchronously with the low-side driver (LVG)—with a diode in series, as shown in *Figure 13*.

An internal charge pump (also shown in *Figure 13*) provides the DMOS driving voltage. The diode connected in series to the DMOS has been added to avoid current flowing in the opposite direction.

6.1 C_{BOOT} selection and charging

To choose the proper C_{BOOT} value the external MOSFET can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the total gate charge of the MOSFET.

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss. It must be:

$$C_{BOOT} >>> C_{EXT}$$

For example, if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF the drop would be 300 mV. If HVG needs to be supplied for a long time, the C_{BOOT} selection also has to take into account the leakage losses.

Another example: HVG's steady state consumption is lower than 200 µA (which is the case for L6385E, L6386E and L6388E, whereas for L6384E and L6387E it is lower than 100 µA). Therefore, if HVG t_{on} is 5 ms, C_{BOOT} has to supply 1 µC to C_{EXT}. This charge on a 1-µF capacitor means a voltage drop of 1 V.

The internal bootstrap driver provides great advantages; it avoids use of the external fast recovery diode (which usually has a high leakage current). This type of structure can only work if V_{OUT} is close to GND (or lower) and while the LVG is ON. The charging time (T_{charge}) of C_{BOOT} is the time it takes for both conditions to be fulfilled and must be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS $R_{DS(on)}$ (typical for L638xE is 125 Ω). At low frequencies this drop is negligible, but when the frequency is increased it must be taken into account.

The following equation is useful to compute the drop on the bootstrap DMOS.

$$V_{drop} = I_{charge} \cdot R_{DS(on)} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} R_{DS(on)}$$

Q_{gate} is the gate charge of the external power MOSFET, $R_{DS(on)}$ is the ON resistance of the bootstrap DMOS, and T_{charge} is the charging time of the bootstrap capacitor.

For example, using a power MOSFET with a total gate charge of 30 nC, the drop on the bootstrap DMOS is about 1 V if T_{charge} is 5 µs.

In fact:

$$V_{drop} = \frac{30\ nC}{5\ \mu s} \cdot 125\ \Omega \approx 0.8\ V$$

V_{drop} must be taken into consideration when the voltage drop on C_{BOOT} is calculated. If the drop is too high or the circuit topology does not provide for a sufficient charging time (like the examples shown in *Figure 18*, *Figure 19* and *Figure 20*), an external diode can be used. This is the reason why the external diode D1 is dotted in *Figure 2*, *Figure 5* and *Figure 8*.

When operating at very low frequencies, the high-side ON time can be very long. The C_{BOOT} voltage can drop because of the steady state consumption of the HGV. To avoid having to use extremely large capacitors (> 1 to 2 µF), an external charge pump can be added (see *Figure 14* as an example). The diodes are signal diodes because the high voltage drops on C1 and C2. It is mandatory that the diodes have a low parasitic capacitance because C1 and C2 have to be greater than the diodes' capacitance. The oscillator has to balance the consumption of the high-voltage side and the minimum frequency is fixed by the values of C1 and C2 (with C1 and C2 = 33 pF -> f > 250-300 kHz). Additionally, the oscillator has to be able to sustain the dV/dt of the OUT pin.

Figure 12. External bootstrap diode: principle schematic

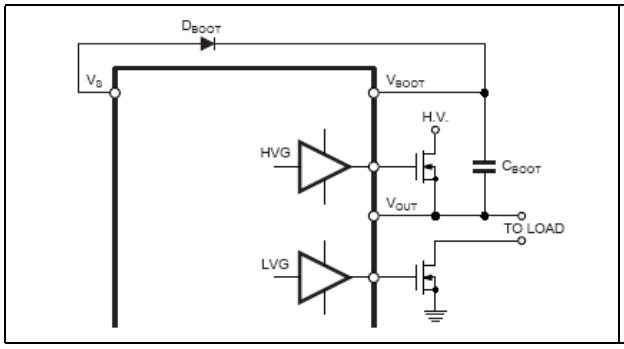


Figure 13. Internal bootstrap diode: principle schematic

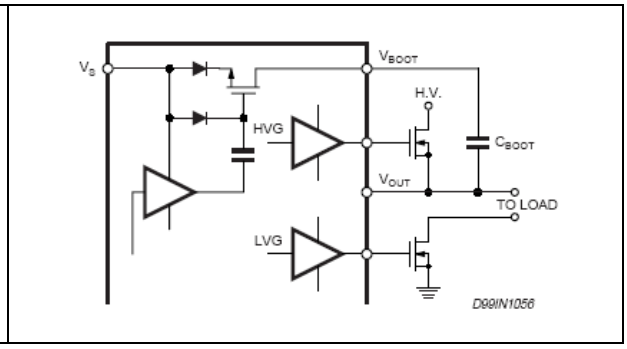
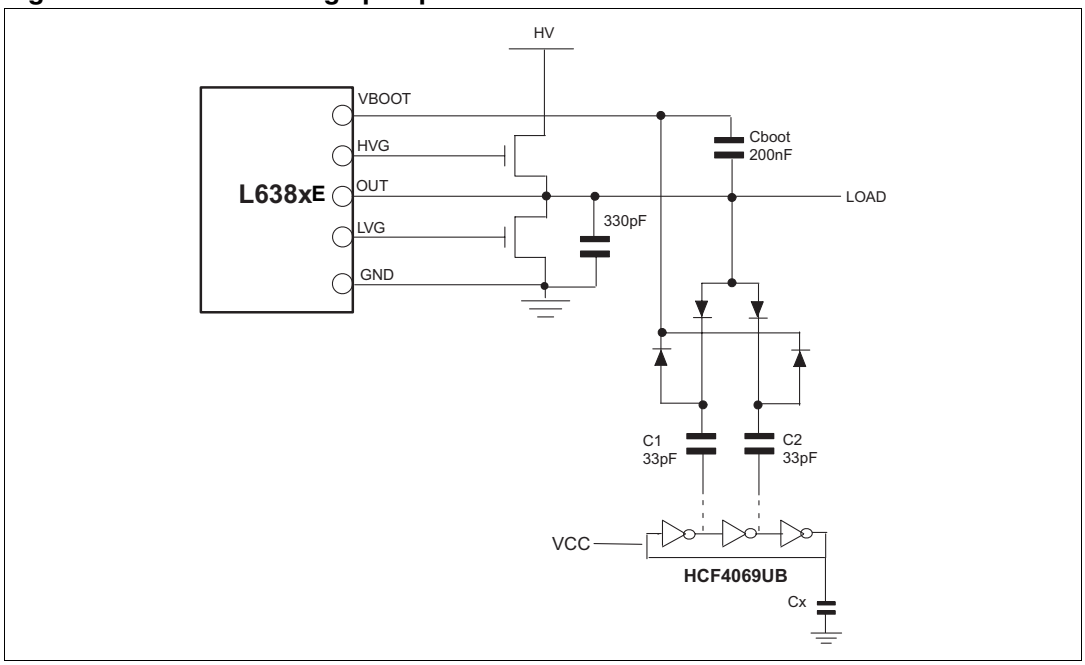


Figure 14. External charge pump



7 Application examples

This section provides several application suggestions that highlight the versatility and flexibility of this family of high- and low-side drivers. Their simplicity and compactness make these devices a cost-effective solution.

For further information on these ICs, refer to the following documents.

- AN1263: "Using the internal bootstrap current capability of the L638xE in driving a six transistor inverter bridge".
- AN1299: "L638xE tricks and tips".

Figure 15. L6384E µC 3-phase motor control

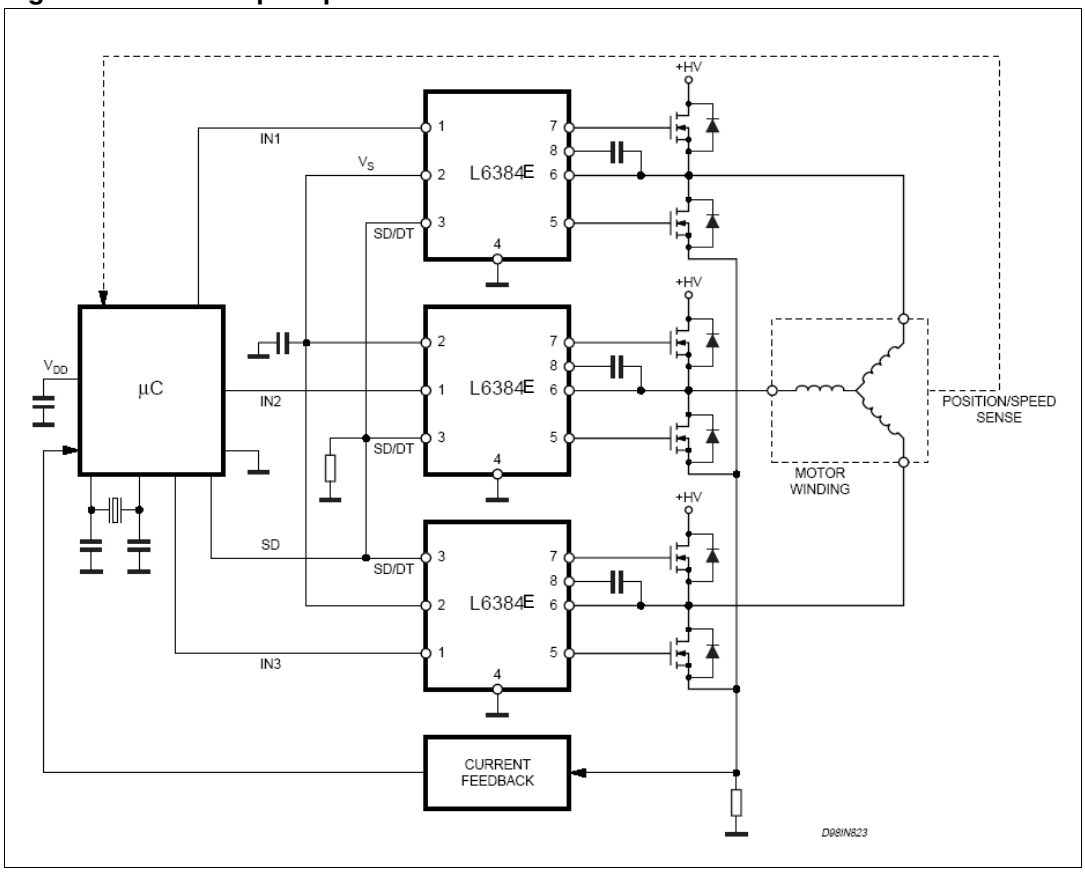


Figure 16. L6384E dimmable lamp ballast

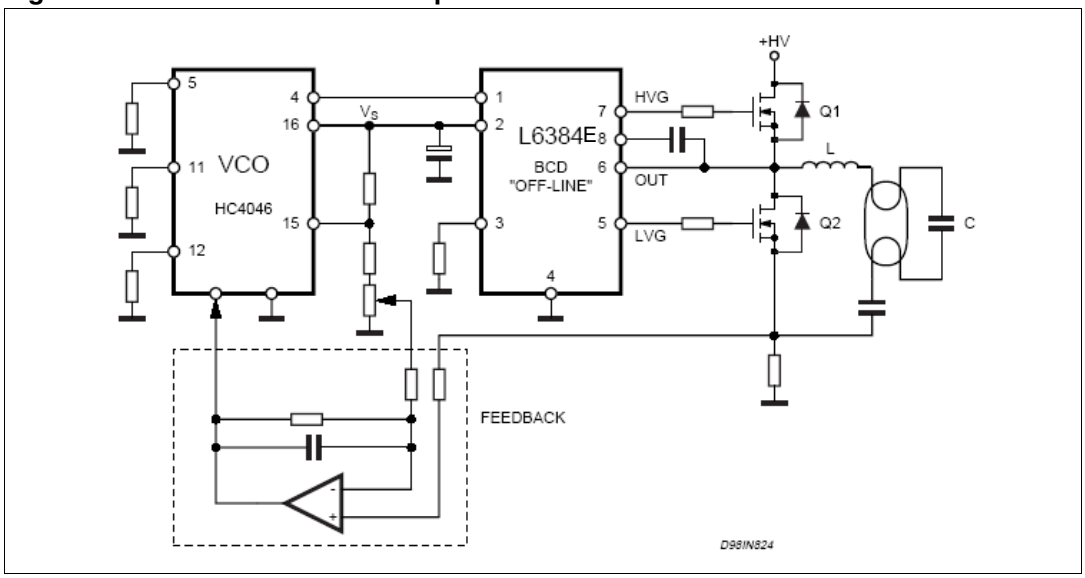


Figure 17. L6384E half bridge converter

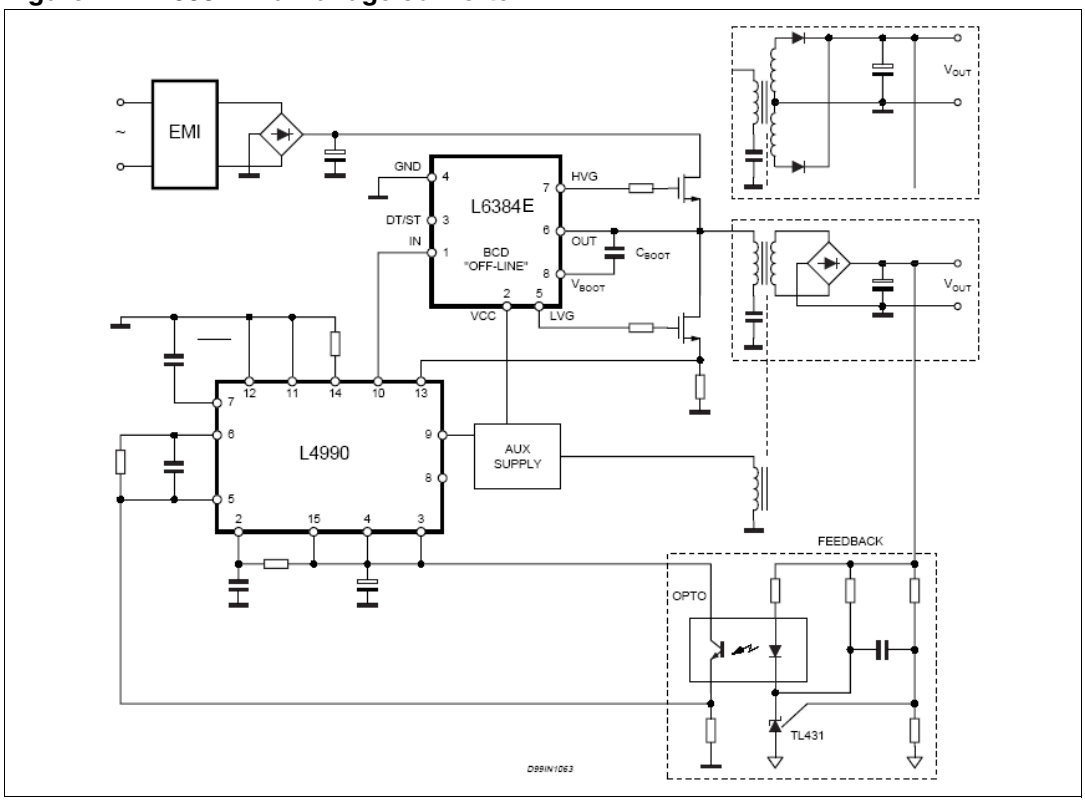


Figure 18. L6385E horizontal deflection stage

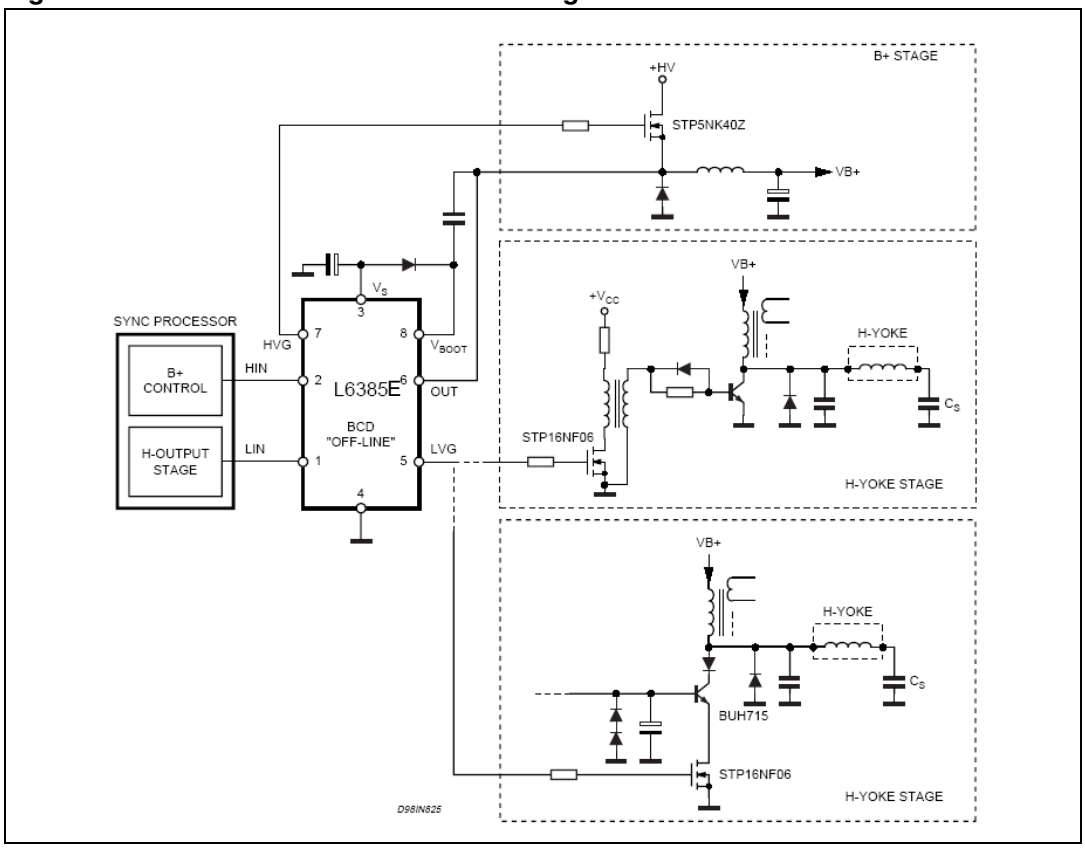


Figure 19. L6385E 2-switch forward converter

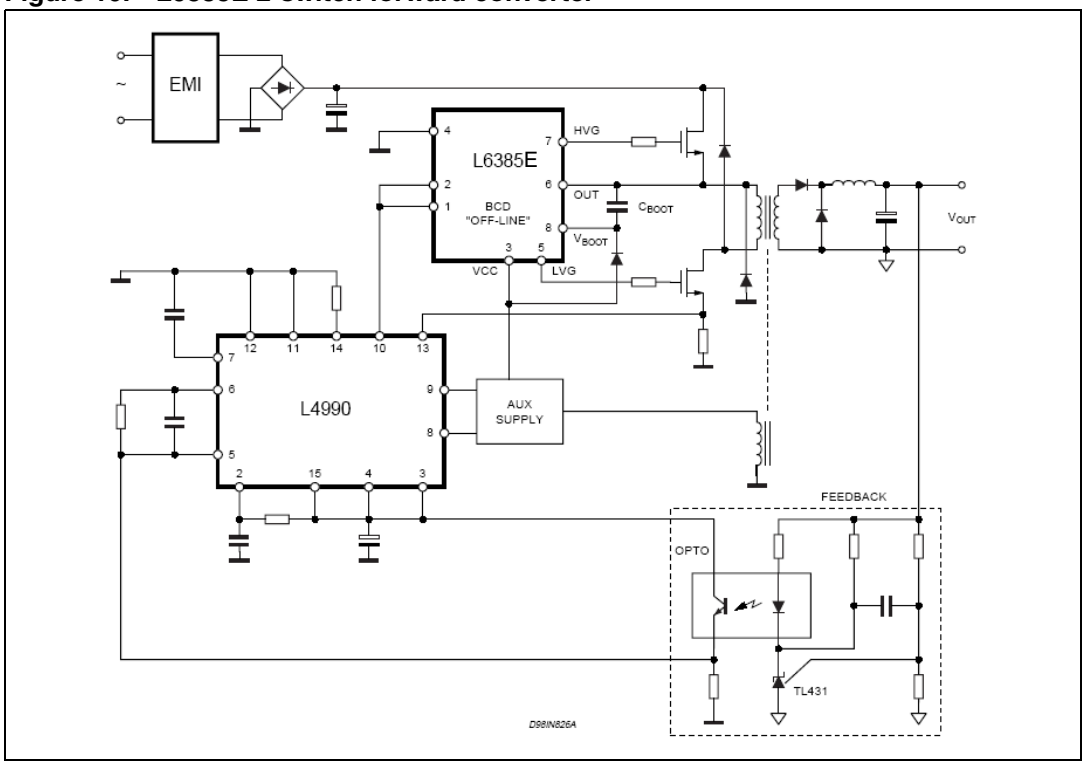


Figure 20. L6385E asymmetrical half bridge

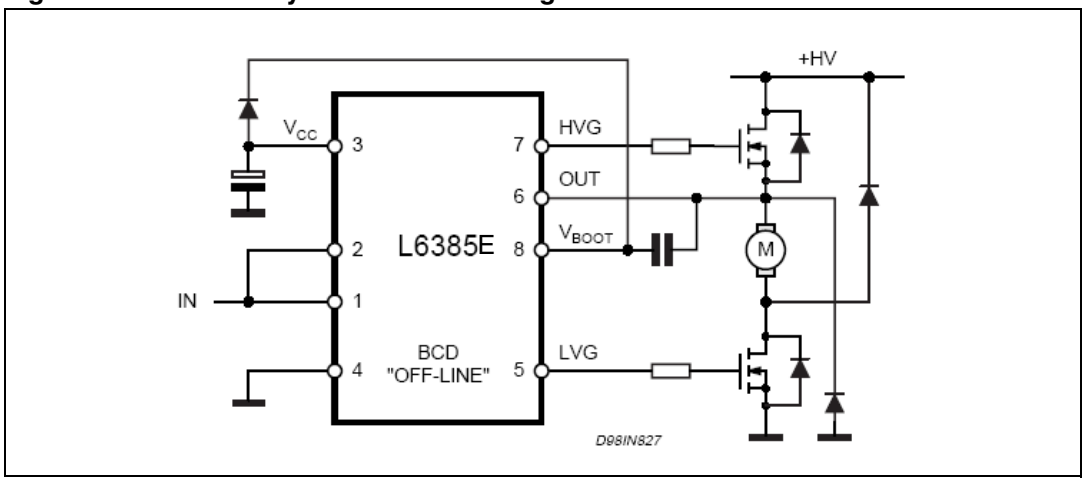
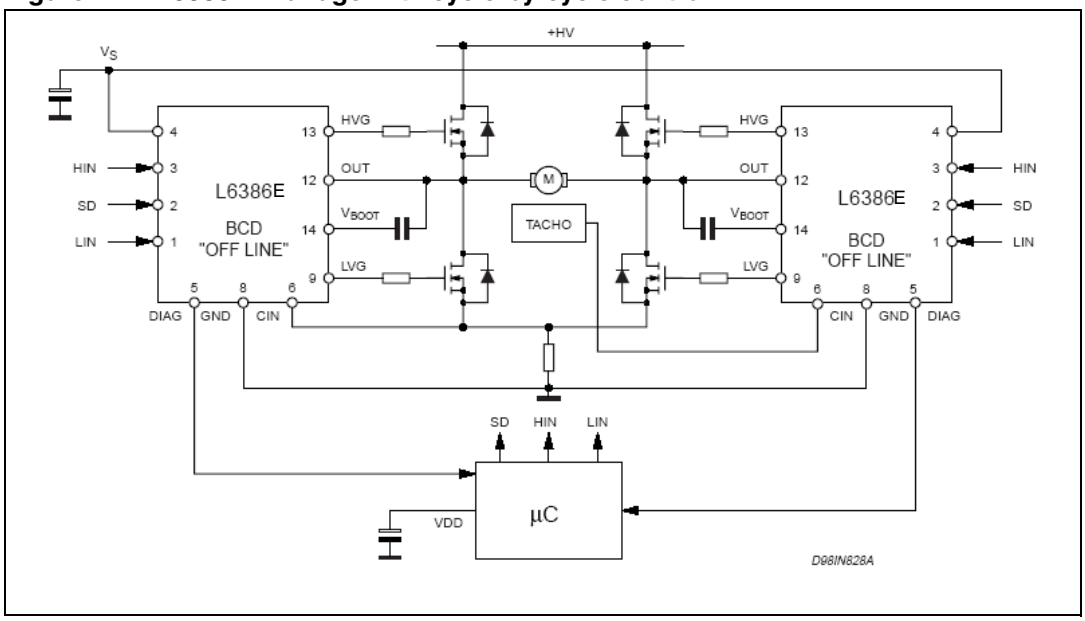


Figure 21. L6386E h-bridge with cycle-by-cycle control



8 Revision history

Table 7. Document revision history

Date	Revision	Changes
09-Sep-2004	6	Minor text changes
17-Feb-2009	7	Added: *Section 5: L6388E* – L6384 replaced by L6384E, L6385 replaced by L6385E, L6386 replaced by L6386E, L6387 replaced by L6387E, L6388 replaced by L6388E, L638x replaced by L638xE.