

**2.5 V or 3.3 V, 200 MHz,
1:10 Clock Distribution Buffer**

Features

- 2.5 V or 3.3 V operation
- 200-MHz clock support
- Two LVCMOS-/LVTTTL-compatible inputs
- Ten clock outputs: drive up to 20 clock lines
- 1× or 1/2× configurable outputs
- Output three-state control
- 250-ps max output-to-output skew
- Pin-compatible with MPC946, MPC9446
- Available in commercial and industrial temperature range
- 32-pin TQFP package

Functional Description

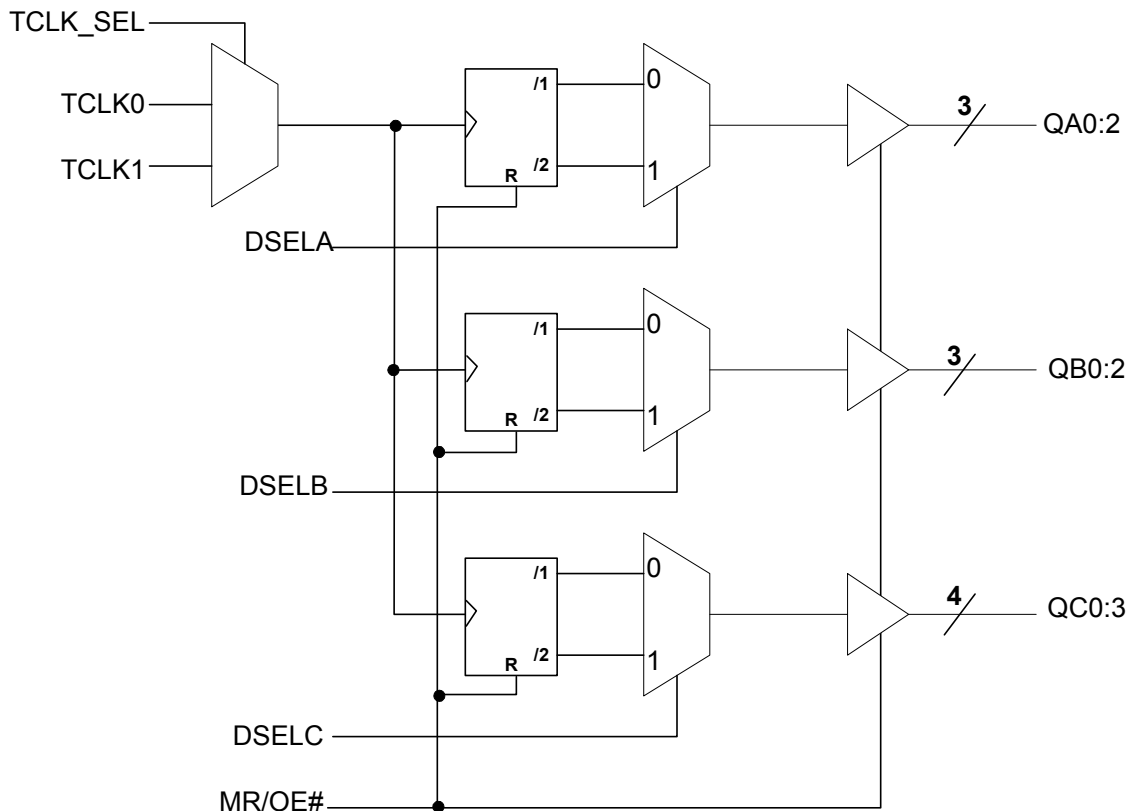
The CY29946 is a low-voltage 200-MHz clock distribution buffer with the capability to select one of two LVCMOS/LVTTTL compatible input clocks. These clock sources can be used to provide for test clocks as well as the primary system clocks. All other control inputs are LVCMOS/LVTTTL compatible. The 10 outputs are LVCMOS or LVTTTL compatible and can drive 50 Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:20.

The CY29946 is capable of generating 1× and 1/2× signals from a 1× source. These signals are generated and retimed internally to ensure minimal skew between the 1× and 1/2× signals. SEL(A:C) inputs allow flexibility in selecting the ratio of 1× to 1/2× outputs.

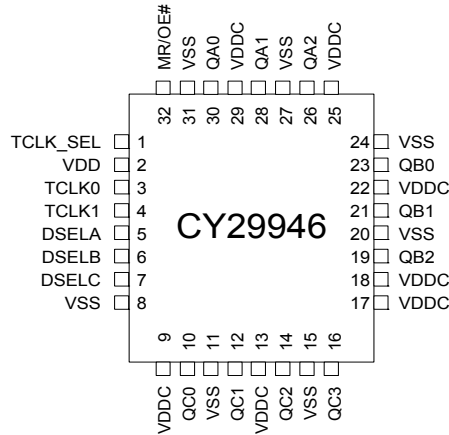
The CY29946 outputs can also be three-stated via MR/OE# input. When MR/OE# is set HIGH, it resets the internal flip-flops and three-states the outputs.

For a complete list of related documentation, [click here](#).

Block Diagram



Pin Configuration



Pin Description

Pin	Name	PWR	I/O ^[1]	Description
3, 4	TCLK(0,1)		I, PU	External Reference/Test Clock Input
26, 28, 30	QA(2:0)	VDDC	O	Clock Outputs
19, 21, 23	QB(2:0)	VDDC	O	Clock Outputs
10, 12, 14, 16	QC(0:3)	VDDC	O	Clock Outputs
5, 6, 7	DSEL(A:C)		I, PD	Divider Select Inputs. When HIGH, selects ÷2 input divider. When LOW, selects ÷1 input divider.
1	TCLK_SEL		I, PD	TCLK Select Input. When LOW, TCLK0 clock is selected and when HIGH TCLK1 is selected.
32	MR/OE#		I, PD	Output Enable Input. When asserted LOW, the outputs are enabled and when asserted HIGH, internal flip-flops are reset and the outputs are three-stated. If more than 1 Bank is being used in /2 Mode, a reset must be performed (MR/OE# Asserted High) after power-up to ensure all internal flip-flops are set to the same state.
9, 13, 17, 18, 22, 25, 29	VDDC			2.5 V or 3.3 V Power Supply for Output Clock Buffers
2	VDD			2.5 V or 3.3 V Power Supply
8, 11, 15, 20, 24, 27, 31	VSS			Common Ground

Note

1. PD = Internal pull-down. PU = Internal pull-up.

Absolute Maximum Conditions^[2]

Maximum Input Voltage Relative to V_{SS}	$V_{SS} - 0.3$ V
Maximum Input Voltage Relative to V_{DD}	$V_{DD} + 0.3$ V
Storage Temperature	-65 °C to +150 °C
Operating Temperature.....	-40 °C to +85 °C
Maximum ESD protection.....	2 kV
Maximum Power Supply	5.5 V
Maximum Input Current.....	±20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Electrical Specifications

$V_{DD} = V_{DDC} = 3.3$ V ± 10% or 2.5 V ± 5%, over the specified temperature range

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage		V_{SS}	–	0.8	V
V_{IH}	Input High Voltage		2.0	–	V_{DD}	V
I_{IL}	Input Low Current ^[3]		–	–	-100	µA
I_{IH}	Input High Current ^[3]		–	–	100	µA
V_{OL}	Output Low Voltage ^[4]	$I_{OL} = 20$ mA	–	–	0.4	V
V_{OH}	Output High Voltage ^[4]	$I_{OH} = -20$ mA, $V_{DD} = 3.3$ V	2.5	–	–	V
		$I_{OH} = -20$ mA, $V_{DD} = 2.5$ V	1.8	–	–	
I_{DDQ}	Quiescent Supply Current		–	5	7	mA
I_{DD}	Dynamic Supply Current	$V_{DD} = 3.3$ V, Outputs @ 100 MHz, CL = 30 pF	–	130	–	mA
		$V_{DD} = 3.3$ V, Outputs @ 160 MHz, CL = 30 pF	–	225	–	
		$V_{DD} = 2.5$ V, Outputs @ 100 MHz, CL = 30 pF	–	95	–	
		$V_{DD} = 2.5$ V, Outputs @ 160 MHz, CL = 30 pF	–	160	–	
Z_{Out}	Output Impedance	$V_{DD} = 3.3$ V	12	15	18	W
		$V_{DD} = 2.5$ V	14	18	22	
C_{in}	Input Capacitance		–	4	–	pF

Thermal Resistance

Parameter ^[5]	Description	Test Conditions	32-pin TQFP	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	65	°C/W
θ_{JC}	Thermal resistance (junction to case)		12	°C/W

Notes

- Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.
- Inputs have pull-up/pull-down resistors that effect input current.
- Driving series or parallel terminated 50 Ω (or 50 Ω to $V_{DD}/2$) transmission lines.
- These parameters are guaranteed by design and are not tested.

AC Electrical Specifications

$V_{DD} = V_{DDC} = 3.3\text{ V} \pm 10\%$ or $2.5\text{ V} \pm 5\%$, over the specified temperature range^[6]

Parameter	Description	Conditions	Min	Typ	Max	Unit
F _{max}	Input Frequency ^[7]	V _{DD} = 3.3 V	–	–	200	MHz
		V _{DD} = 2.5 V	–	–	170	
T _{pd}	TTL_CLK To Q Delay ^[7]		5.0	–	11.5	ns
F _{outDC}	Output Duty Cycle ^[7, 8]	Measured at V _{DD} /2	45	–	55	%
t _{pZL} , t _{pZH}	Output enable time (all outputs)		2	–	10	ns
t _{pLZ} , t _{pHZ}	Output disable time (all outputs)		2	–	10	ns
T _{skew}	Output-to-Output Skew ^[7, 9]		–	150	250	ps
T _{skew(pp)}	Part-to-Part Skew ^[10]		–	2.0	4.5	ns
T _r /T _f	Output Clocks Rise/Fall Time ^[9]	0.8 V to 2.0 V, V _{DD} = 3.3 V	0.10	–	1.0	ns
		0.6 V to 1.8 V, V _{DD} = 2.5 V	0.10	–	1.3	

Notes

6. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
7. Outputs driving 50Ω transmission lines.
8. 50% input duty cycle.
9. See [Figure 1 on page 5](#).
10. Part-to-Part skew at a given temperature and voltage.

Figure 1. LVCMOS_CLK CY29946 Test Reference for $V_{CC} = 3.3\text{ V}$ and $V_{CC} = 2.5\text{ V}$

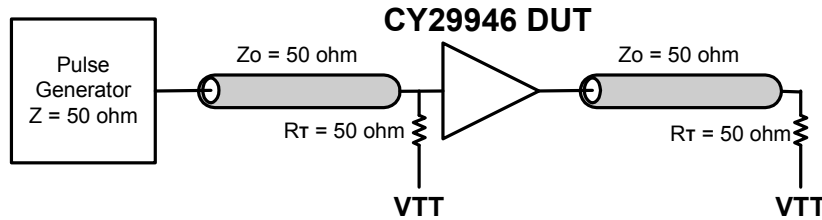


Figure 2. LVCMOS Propagation Delay (T_{PD}) Test Reference

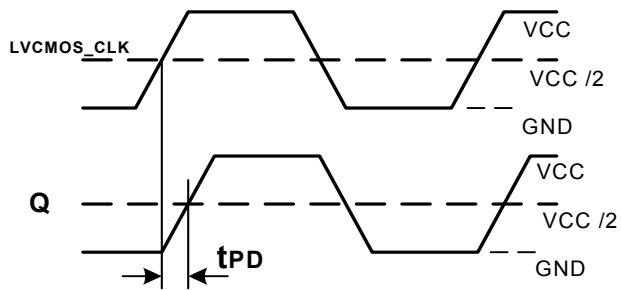


Figure 3. Output Duty Cycle (F_{outDC})

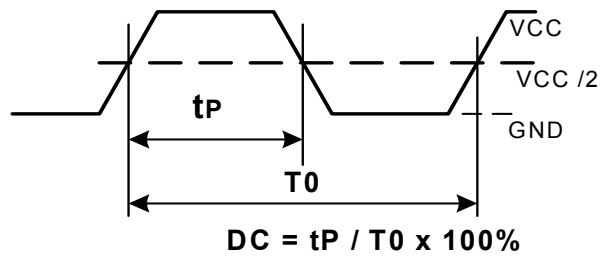
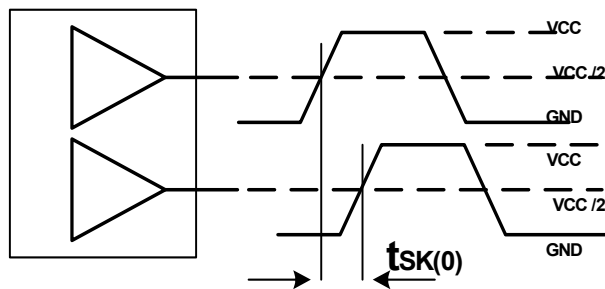


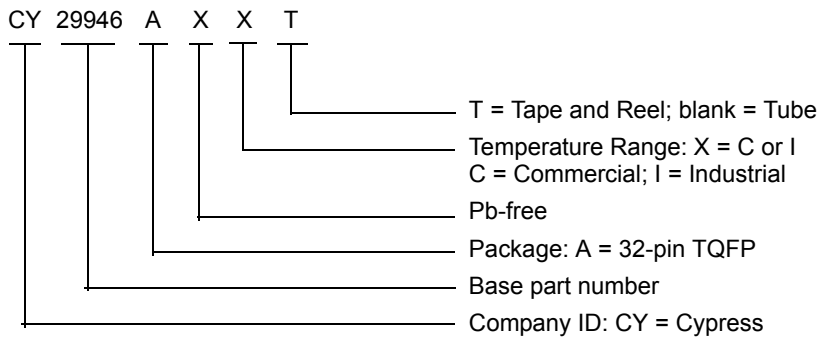
Figure 4. Output-to-Output Skew $t_{sk(0)}$



Ordering Information

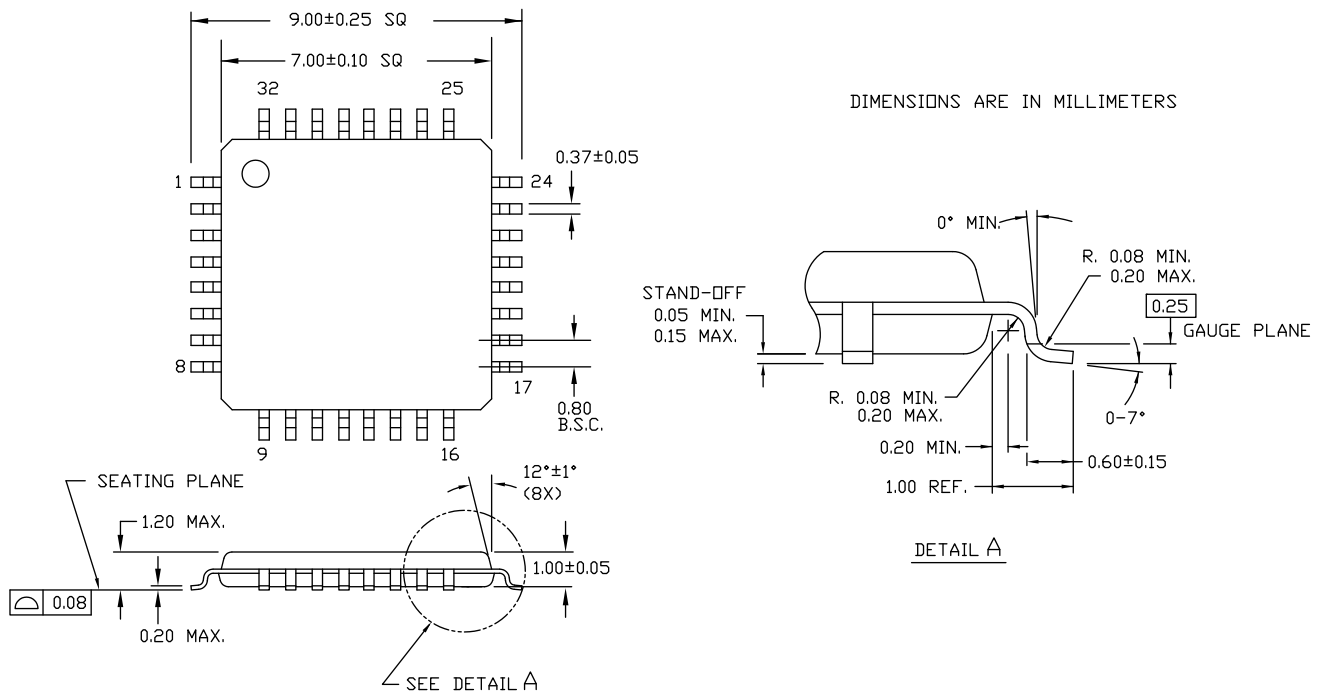
Part Number	Package Type	Production Flow
CY29946AXC	32-pin TQFP	Commercial, 0 °C to +70 °C
CY29946AXCT	32-pin TQFP – Tape and Reel	Commercial, 0 °C to +70 °C
CY29946AXI	32-pin TQFP	Industrial, -40 °C to +85 °C
CY29946AXIT	32-pin TQFP – Tape and Reel	Industrial, -40 °C to +85 °C

Ordering Code Definitions



Package Drawing and Dimensions

Figure 5. 32-pin TQFP 7 × 7 × 1.0 mm A3210



51-85063 *E

Acronyms

Acronym	Description
ESD	electrostatic discharge
I/O	input/output
LVC MOS	low voltage complementary metal oxide semiconductor
LV TTL	low-voltage transistor-transistor logic
TQFP	thin quad flat pack

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kV	kilovolt
MHz	megahertz
μA	microampere
mA	milliampere
mm	millimeter
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY29946, 2.5 V or 3.3 V, 200 MHz, 1:10 Clock Distribution Buffer Document Number: 38-07286				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	111097	02/07/02	BRK	New data sheet
*A	116780	08/15/02	HWT	Added the commercial temperature range in the Ordering Information
*B	122878	12/22/02	RBI	Added power-up requirements to Maximum Ratings
*C	130007	10/15/03	RGL	Fixed the block diagram. Fixed the MK/OE# description in the pin description table.
*D	131375	11/21/03	RGL	Updated document history page (revision *C) to reflect changes that were not listed.
*E	221587	See ECN	RGL	Minor Change: Moved up the word Block Diagram in the first page.
*F	2899714	03/26/10	BRIJ / CXQ	Removed inactive parts from the ordering table. Updated package diagram
*G	3254185	05/11/2011	CXQ	Added Ordering Code Definitions . Added Acronyms and Units of Measure . Updated to new template.
*H	4389717	05/30/2014	XHT	Updated Package Drawing and Dimensions : spec 51-85063 – Changed revision from *C to *D. Completing Sunset Review.
*I	4586288	12/03/2014	XHT	Updated Functional Description : Added “For a complete list of related documentation, click here .” at the end.
*J	5270507	05/13/2016	PSR	Added Thermal Resistance . Updated Package Drawing and Dimensions : spec 51-85063 – Changed revision from *D to *E. Updated to new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Lighting & Power Control	cypress.com/powerpsoc
Memory	cypress.com/memory
PSoC	cypress.com/psoc
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless/RF	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

Cypress Developer Community

[Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2002-2016. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.